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# XPX120P06TU

Halogen-Free

### -60V P-Channel Enhancement Mode MOSFET

RoHS

H

### Features

- Advanced HEFET Technology
- Ultra Low On-Resistance
- Excellent QgxRDS(on) Product
- 100% avalanche tested
- 175°C Operating Temperature
- Lead Free and Green Devices Available (RoHS Comp.

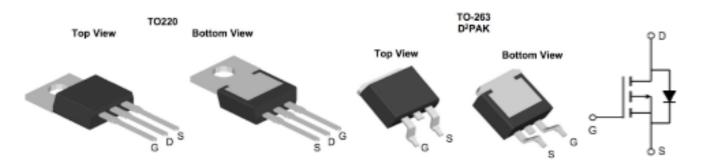
Applications



- Uninterruptible Power Supplies
- DC/DC converter
- General Purpose Applications

V<sub>DS</sub> = -60V I<sub>D</sub> =-120A

R<sub>DS(ON)</sub> <6.5mΩ @ V<sub>GS</sub>=10V



Product ID	Pack	Marking	Qty(PCS)
XPX120P06TU	TO-220-3L	XPX120P06TU XXX YYYY	1000
XPX120P06TT	TO-263-3L	XPX120P06TT XXX YYYY	800

#### Absolute Maximum Ratings (Tc=25°Cunless otherwise noted)

Symbol	Parameter	Rating	Units
Vds	Drain-Source Voltage	-60	V
Vgs	Gate-Source Voltage	±20	V
I₀@Tc=25°C	Continuous Drain Current, -V <sub>GS</sub> @ -10V <sup>1</sup>	-120	А
I₀@Tc=100°C	Continuous Drain Current, -V <sub>GS</sub> @ -10V <sup>1</sup>	-65	А
Ідм	Pulsed Drain Current <sup>2</sup>	-300	А
EAS	Single Pulse Avalanche Energy <sup>3</sup>	650	mJ
AS	Avalanche Current	80	A
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation <sup>4</sup>	142	W
Тѕтс	Storage Temperature Range	-55 to 150	°C
TJ	Operating Junction Temperature Range	-55 to 150	°C
R <sub>0</sub> JA	Thermal Resistance Junction-Ambient <sup>1</sup>	0.88	°C/W
R <sub>θ</sub> JC	Thermal Resistance Junction-Case <sup>1</sup>	60	°C/W



#### Electrical Characteristics (Tc=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =-250uA	-60	-72		V
$\triangle BVDSS / \triangle TJ$	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25 $^\circ\!\mathrm{C}$ , I_D=-1mA		-0.035		V/℃
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-10V , I <sub>D</sub> =-20A		6.5	8.5	mΩ
		V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-15A		7.8	10	
VGS(th)	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =-250uA	-1.2	-1.6	-2.5	V
$ riangle V_{GS(th)}$	V <sub>GS(th)</sub> Temperature Coefficient	VGS-VDS, ID2000A		4.28		mV/℃
IDSS	Dursin Source Lookene Current	$V_{\text{DS}}\text{=-60V}$ , $V_{\text{GS}}\text{=}0\text{V}$ , $T_{\text{J}}\text{=}25^\circ\!\!\mathbb{C}$			1	uA
1033	Drain-Source Leakage Current	$V_{\text{DS}}\text{=-60V}$ , $V_{\text{GS}}\text{=}0\text{V}$ , $T_{\text{J}}\text{=}55^\circ\!\!\mathbb{C}$			5	uA
IGSS	Gate-Source Leakage Current	$V_{GS}$ =±20V , $V_{DS}$ =0V			±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =-5V , I <sub>D</sub> =-20A		18		S
Rg	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz		4.0		Ω
Qg	Total Gate Charge (-4.5V)			141		
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =-48, V <sub>GS</sub> =-10V , I <sub>D</sub> =-5		17		nC
Q <sub>gd</sub>	Gate-Drain Charge			28.6		
Td(on)	Turn-On Delay Time			70		
Tr	Rise Time	$V_{DD}$ =-48, $V_{GS}$ =-10V,		205		
Td(off)	Turn-Off Delay Time	R <sub>G</sub> =6,I <sub>D</sub> =-1A		402		ns
T <sub>f</sub>	Fall Time			402		
Ciss	Input Capacitance			8610		
Coss	Output Capacitance	V <sub>DS</sub> =-25V , V <sub>GS</sub> =0V , f=1MHz		486		pF
Crss	Reverse Transfer Capacitance			288		
ls	Continuous Source Current <sup>1,5</sup>				-10	А
ISM	Pulsed Source Current <sup>2,5</sup>	$V_G = V_D = 0V$ , Force Current			-144	А
VSD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =-1A , TJ=25℃			-1.2	V

Note :

1. The data tested by surface mounted on a 1 inch 2  $\,$  FR-4 board with 2OZ copper.

2. The data tested by pulsed , pulse width  $\,\leq\,$  300us , duty cycle  $\,\leq\,$  2%

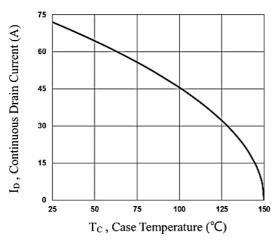
3 The EAS data shows Max. rating . The test condition is VDD =-48V,VGS =-10V,L=0.1mH,IAS =-80A

 $4\,{\ensuremath{\scriptstyle \sim}}$  The power dissipation is limited by  $150\,{\ensuremath{\scriptstyle \odot}}$  junction temperature

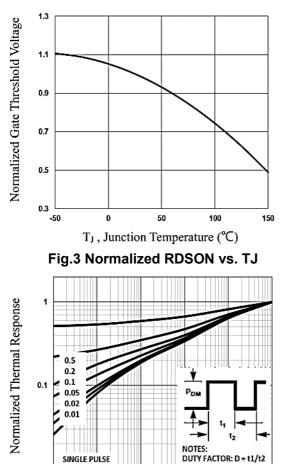
5. The data is theoretically the same as I D and I DM, in real applications, should be limited by total power dissipation.

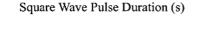


### **Typical Characteristics**



#### Fig.1Typical Output Characteristics





0.1

1

10



0.01

0.01

0.0001

0.001

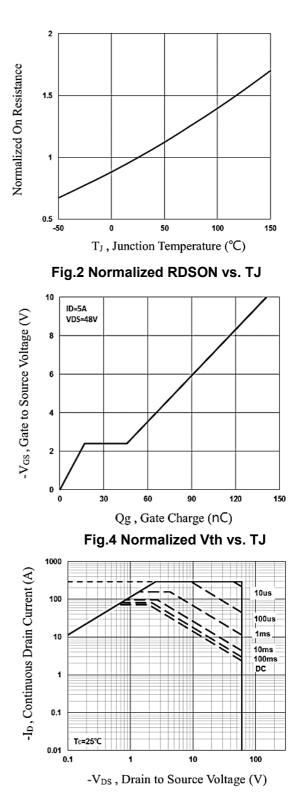
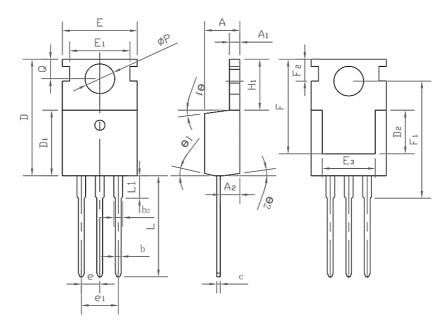


Fig.6 Maximum Safe Operation Area



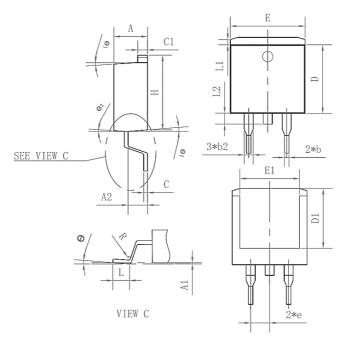
# Package Mechanical Data-TO-220-3L-SLK



		Common		
Symbol		mm		
	Mim	Nom	Max	
A	4.27	4.57	4.87	
A1	1.15	1.30	1.45	
A2	2.10	2.40	2.70	
b	0.70	0.80	1.00	
b2	1.17	1.27	1.50	
D	0.40	0.50	0.65	
D1	8.80	9.10	9.40	
D2	5.70	6.70	7.00	
E	9.70	10.00	10.30	
E1	-	8.70	-	
E2	9.63	10.00	10.35	
E3	7.00	8.00	8.40	
е		0.37		
e1		0.10		
H1	6.00	6.50	6.85	
L	12.75	13.50	13.90	
L1	-	3.10	3.40	
Фр	3.45	3.60	3.75	
Q	2.60	2.80	3.00	
θ1	4°	7°	10°	
θ2	0°	3°	6°	
F	13.30	13.50	13.70	
F1	15.50	15.90	16.30	
F2	2.80	3.00	3.20	



# Package Mechanical Data-TO-263-3L-SLK



	Common mm		
Symbol			
-	Mim	Nom	Max
A	4.35	4.47	4.60
A1	0.09	0.10	0.11
A2	2.30	2.40	2.70
b	0.70	0.80	1.00
b2	1.25	1.36	1.50
С	0.45	0.50	0.65
C1	1.29	1.30	9.40
D	9.10	9.20	9.30
D1	7.90	8.00	8.10
E	9.85	10.00	10.20
E1	7.90	8.00	8.10
Н	15.30	15.50	15.70
е	-	2.54	-
L	2.34	2.54	2.74
L1	1.00	1.10	1.20
L2	1.30	1.40	1.50
R	0.24	0.25	0.26
θ	0°	4°	8°
Θ1	4°	7°	10°
Θ2	0°	3°	6°



#### Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	<b>245℃±5</b> ℃	5sec±1sec
Pb-Free device	<b>260</b> ℃ <b>+0/-5</b> ℃	5sec <del>±</del> 1sec



This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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