650V N-Channel Enhancement Mode MOSFET

Description

TheXPX15N65FD MOSFET family

that is utilizing charge balance technology for extremely

low on-resistance and low gate charge performance.

APJ14N65F/P/T is suitable for applications which require

superior power density and outstanding efficiency

General Features

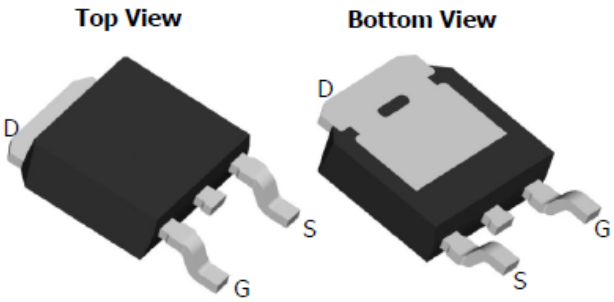
V_{DS} = 650V IDM =15A

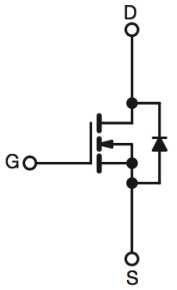
$R_{DS(ON)}$ < 560mΩ @ V_{GS}=10V

Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)





N-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
XPX15N65FD	TO-252-3L	XPX15N65FD XXX YYYY	2500

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Value	Unit
VDSS	Drain-Source Voltage (V_{GS} = 0V)	650	V
ID	Continuous Drain Current	8	A
IDM	Pulsed Drain Current (note1)	15	A
VGS	Gate-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy (note2)	125	mJ
P_D	Power Dissipation (T_C = 25ºC)	25.5	W
TJ, Tstg	Operating Junction and Storage Temperature Range	-55~+150	ºC
RthJC	Thermal Resistance, Junction-to-Case	4.9	ºC/W
RthJA	Thermal Resistance, Junction-to-Ambient	49	ºC/W

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Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain to source breakdown voltage	V_{GS}=0V, I_D=250uA	650	700	--	V
ΔBV_{DSS} / ΔTJ	Breakdown voltage temperature coefficient	I_D=250uA, referenced to 25°C	--	0.7	--	V/°C
IDSS	Drain to source leakage current	V_{DS}=650V, V_{GS}=0V	--	--	1	uA
		V_{DS}=520V, T_C=125°C	--	--	50	uA
IGSS	Gate to source leakage current, forward	V_{GS}=30V, V_{DS}=0V	--	--	100	nA
	Gate to source leakage current, reverse	V_{GS}=-30V, V_{DS}=0V	--	--	-100	nA
VGS(TH)	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250uA	2.5	3.3	4.5	V
RDS(ON)	Drain to source on state resistance	V_{GS}=10V, I_D =3.2A	--	560	650	mΩ
Ciss	Input capacitance	V_{GS}=0V, V_{DS}=100V, f=1MHz	--	439	--	pF
Coss	Output capacitance		--	19.7	--	
Crss	Reverse transfer capacitance		--	1.32	--	
td(on)	Turn on delay time	V_{DS}=400V, I_D=3.2A, R_G=4.7Ω , V_{GS}=10V	--	84.8	--	ns
tr	Rising time		--	25.2	--	
td(off)	Turn off delay time		--	227.6	--	
t_f	Fall time		--	26.8	--	
Q_g	Total gate charge	V_{DS}=480V, V_{GS}=10V, I_D=3.2A	--	11		nC
Q_{gs}	Gate-source charge		--	2.1	--	
Q_{gd}	Gate-drain charge		--	5.6	--	
IS	Continuous source current	Integral reverse p-n Junction diode in the MOSFET	--	--	11	A
ISM	Pulsed source current		--	--	44	A
VSD	Diode forward voltage drop.	I_S=3.2A, V_{GS}=0V	--	0.7	1.5	V
T_{rr}	Reverse recovery time	I_S=3.2A, V_{GS}=0V, Vdd=400V, dI_F/dt=100A/us,	--	313	--	ns
Qrr	Reverse recovery Charge		--	0.877	--	uC

Note :

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
2、The EAS data shows Max. rating . L=0.5mH, IAS =3.2A, VDD =50V, RG=25Ω
3、The test condition is Pulse Test: ISD ≤ ID, di/dt = 100A/us, VDD≤ BVDSS, Starting at TJ =25℃
4、The power dissipation is limited by 150℃ junction temperature
5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

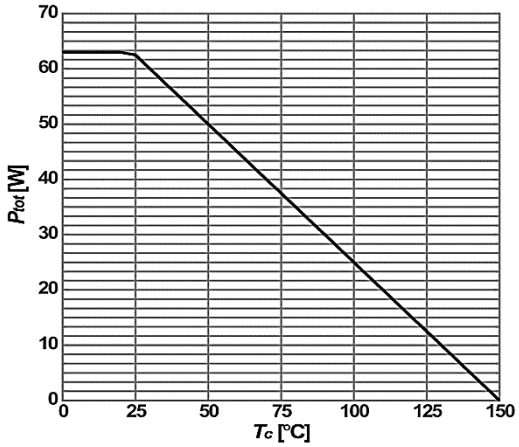

Figure1: Power dissipation (Non FullPAK)

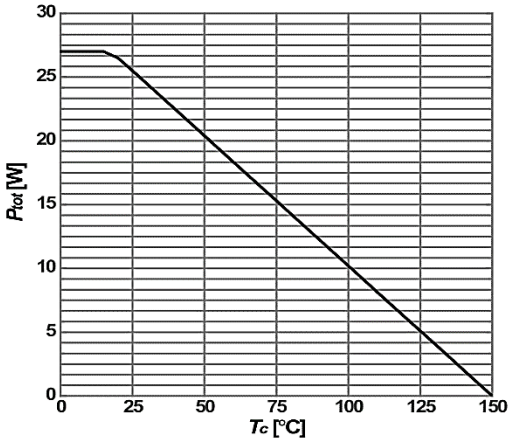

Figure2: Power dissipation (FullPAK)

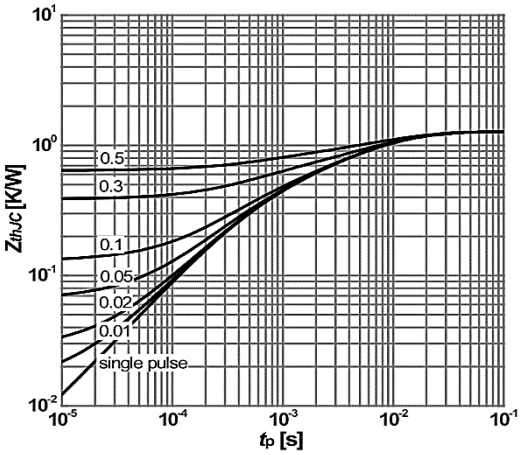

Figure3:Max. transient thermal impedance
Z_{thJC}=f(t_p); parameter: D= t_p/T

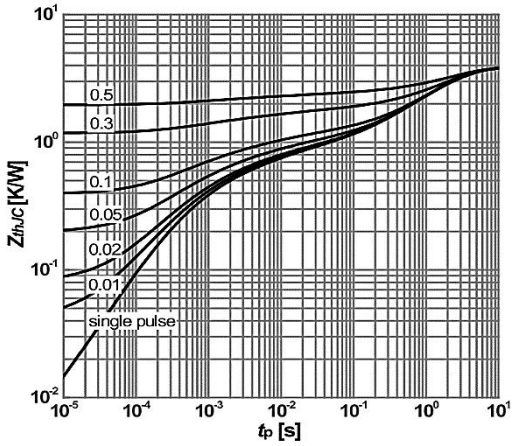

Figure4:Max. transient thermal impedance
Z_{thJC}=f(t_p); parameter: D= t_p/T

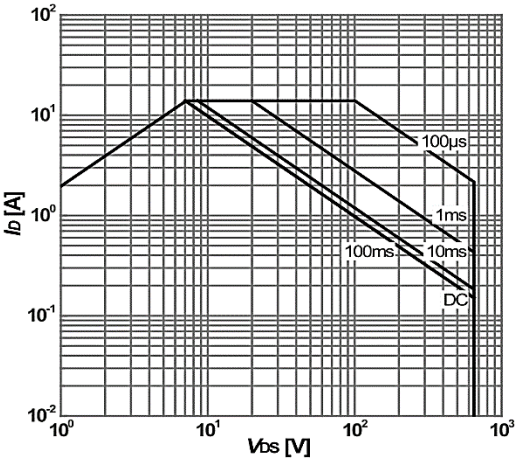

Figure5: Safe operating area (Non FullPAK)
I_D=f(V_{DS}); T_j=25°C; D=0; parameter: t_p

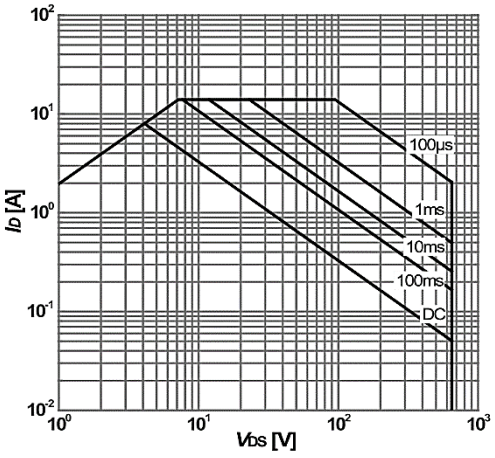

Figure6: Safe operating area (FullPAK)
I_D=f(V_{DS}); T_j=25°C; D=0; parameter: t_p

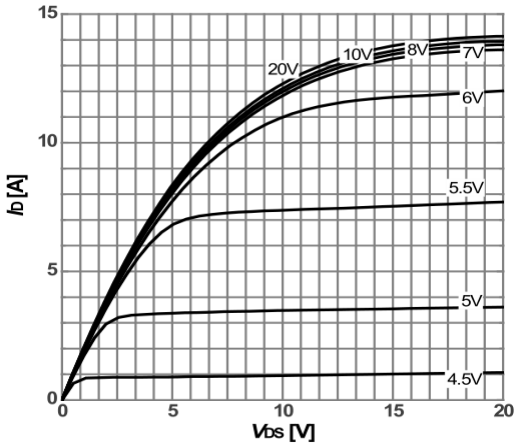

Figure 7: Typ. outp ut characteristics

$I_D=f(V_{DS})$; $T_j=25°C$; parameter: V_{GS}

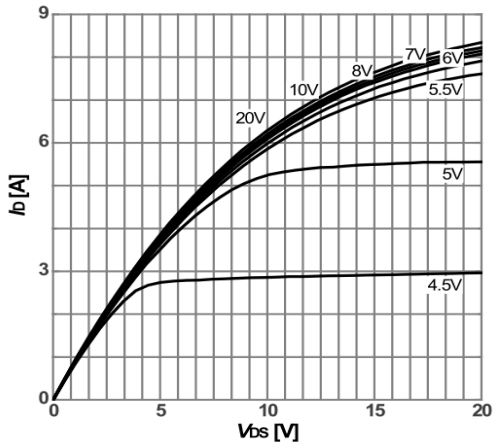

Figure8 : Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=125°C$; parameter: V_{GS}

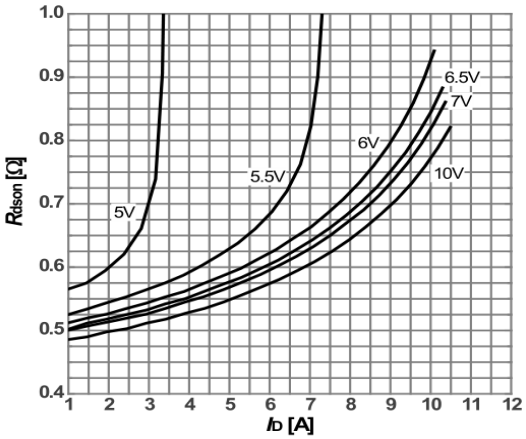

Figure9 : Typ. drain-source on-state resistance

$R_{DS}(on)=f(I_D)$; $T_j=25°C$; parameter: V_{GS}

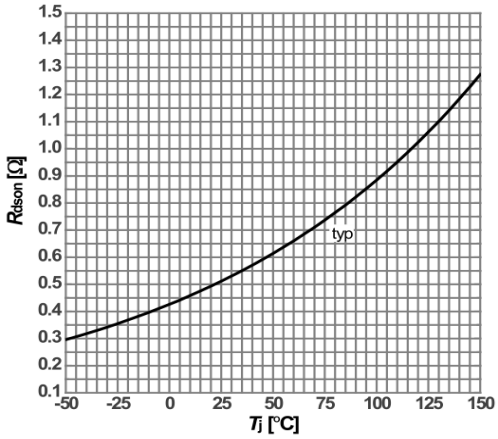

Figure 10: drain -source on-state resistance

$R_{DS}(on)=f(T_j)$; $I_D=3.2A$; $V_{GS}=10V$

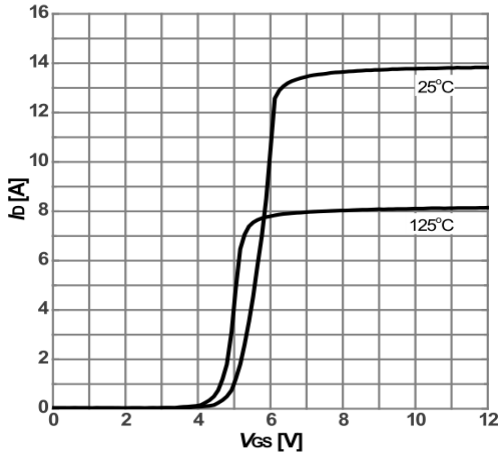

Figure 11: Type. transfer characteristics

$I_D=f(V_{GS})$; $V_{DS}=20V$; parameter: T_j

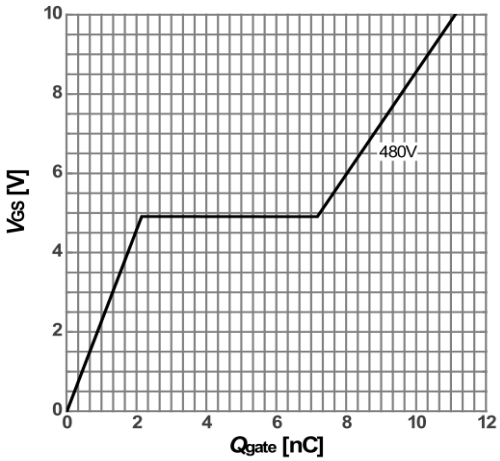

Figure 12: Type. gate charge

$V_{GS}=f(Q_{gate})$; $I_D=3.2A$ pulsed; $V_{DS}=480V$

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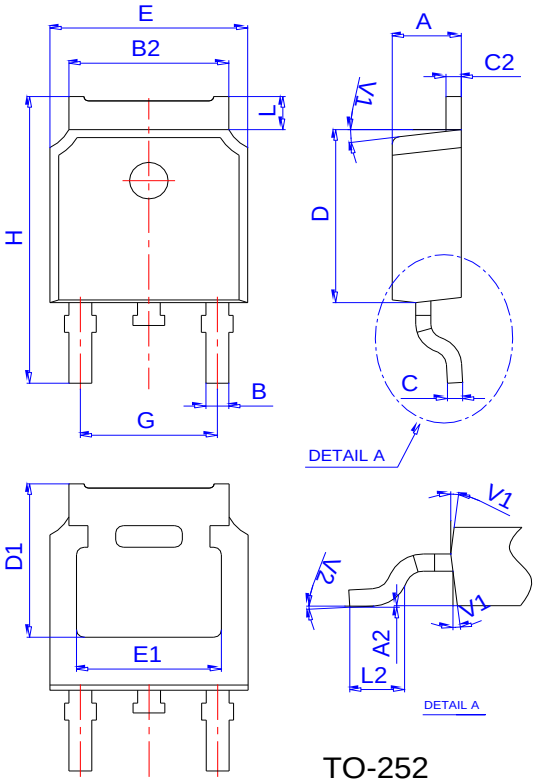
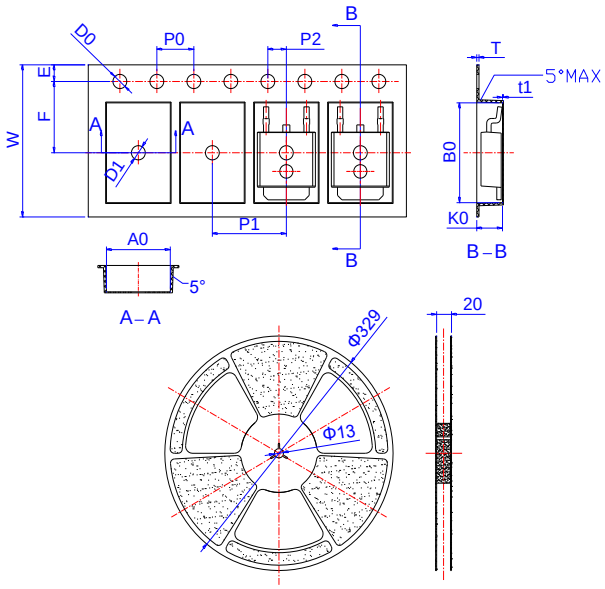
Package Mechanical Data:TO-252-3L



TO-252

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Reel Spectification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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