# 100V N-ChannelEnhancement Mode Power MOSFET

## Description

The XPX18N10XE uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

$V_{DS}$ =100V,$I_D$ =18A

$R_{DS(ON)}$=65mΩ (typ) @ $V_{GS}$=10V

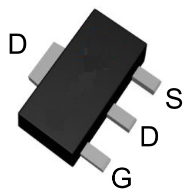
$R_{DS(ON)}$=85mΩ (typ) @ $V_{GS}$=4.5V

## General Features

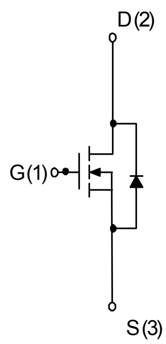
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high $E_{AS}$
- Excellent package for good heat dissipation

## Application

- PWM
- Load Switching




Top View SOT-89




## Package Marking and Ordering Information

| Device Marking | Device | Device Package | Reel Size | Tape width | Quantity |
|---|---|---|---|---|---|
| XPX18N10XE | XPX18N10XE | SOT89-3 | - | - | - |

## Absolute Maximum Ratings ($T_C$=25℃unless otherwise noted)

| Parameter | Symbol | Limit | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 100 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | V |
| Drain Current-Continuous | $I_D$ | 18 | A |
| Drain Current-Continuous($T_C$=100℃) | $I_D$ (100℃) | 10 | A |
| Pulsed Drain Current | $I_{DM}$ | 68 | A |
| Maximum Power Dissipation | $P_D$ | 45 | W |
| Single pulse avalanche energy (Note 5) | $E_{AS}$ | 200 | mJ |
| Operating Junction and Storage Temperature Range | $T_J$,$T_{STG}$ | -55 To 175 | ℃ |
| Thermal Resistance,Junction-to-Case(Note 2) | $R_{θJC}$ | 3.0 | ℃/W |

## Electrical Characteristics ($T_C$=25℃unless otherwise noted)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$=0V $I_D$=250μA | 100 | 110 | - | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=100V,$V_{GS}$=0V | - | - | 1 | μA |
| Gate-Body Leakage Current | $I_{GSS}$ | $V_{GS}$=±20V,$V_{DS}$=0V | - | - | ±100 | nA |
| **On Characteristics** (Note 3) | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$,$I_D$=250μA | 1.2 | 1.8 | 2.5 | V |
| Drain-Source On-State Resistance | $R_{DS(ON)}$ | $V_{GS}$=10V, $I_D$=18A | - | 65 | 75 | mΩ |
| | | $V_{GS}$=4.5V, $I_D$=10A | - | 72 | 86 | |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$=5V,$I_D$=10A | - | 10 | - | S |
| **Dynamic Characteristics** (Note4) | | | | | | |
| Input Capacitance | $C_{lss}$ | $V_{DS}$=50V,$V_{GS}$=0V, F=1.0MHz | - | 880 | - | PF |
| Output Capacitance | $C_{oss}$ | | - | 46 | - | PF |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 33 | - | PF |
| **Switching Characteristics** (Note 4) | | | | | | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$=50V, $R_L$=6.4Ω $V_{GS}$=10V,$R_G$=3Ω | - | 15 | - | nS |
| Turn-on Rise Time | $t_r$ | | - | 5 | - | nS |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 25 | - | nS |
| Turn-Off Fall Time | $t_f$ | | - | 7 | - | nS |
| Total Gate Charge | $Q_g$ | $V_{DS}$=50V,$I_D$=18A, $V_{GS}$=10V | - | 22.3 | | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 2.87 | - | nC |
| Gate-Drain Charge | $Q_{gd}$ | | - | 6.14 | - | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| Diode Forward Voltage (Note 3) | $V_{SD}$ | $V_{GS}$=0V,$I_S$=18A | - | - | 1.2 | V |
| Diode Forward Current (Note 2) | $I_S$ | | - | - | 18 | A |

## Notes:

**1.** Repetitive Rating: Pulse width limited by maximum junction temperature.
**2.** Surface Mounted on FR4 Board, t ≤ 10 sec.
**3.** Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
**4.** Guaranteed by design, not subject to production
**5.** EAS condition：Tj=25℃,$V_{DD}$=50V,$V_G$=10V,L=0.5mH,Rg=25Ω

## Typical Electrical and Thermal Characteristics (Curves)

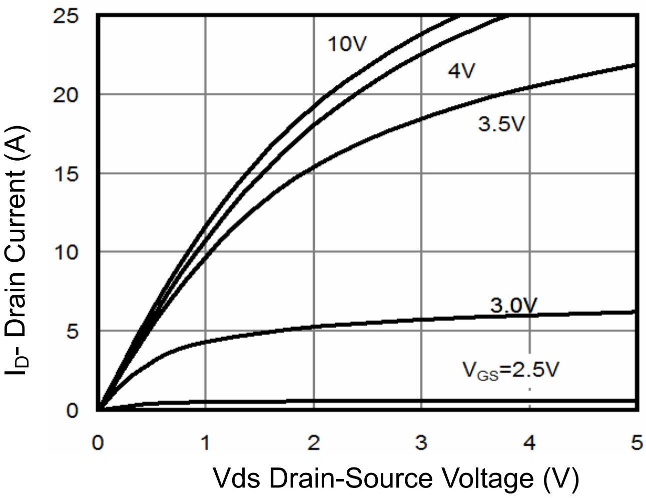



**Figure 1 Output Characteristics**

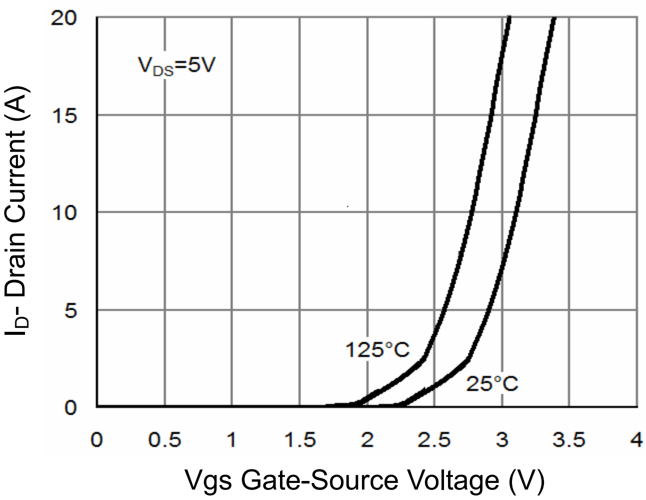



**Figure 2 Transfer Characteristics**

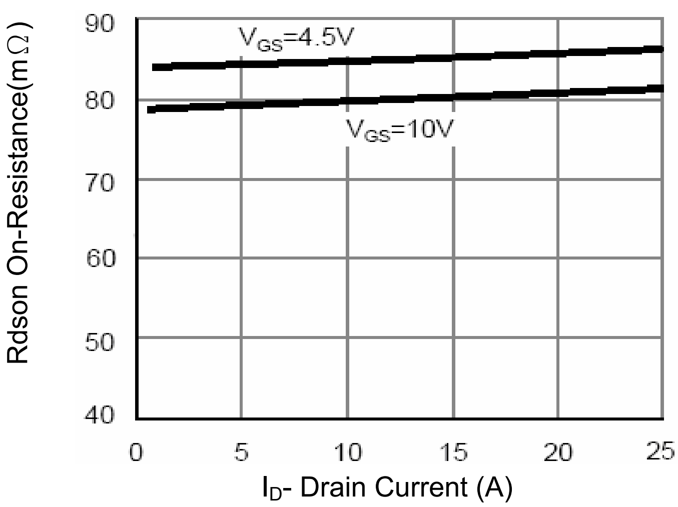



**Figure 3 Rdson- Drain Current**

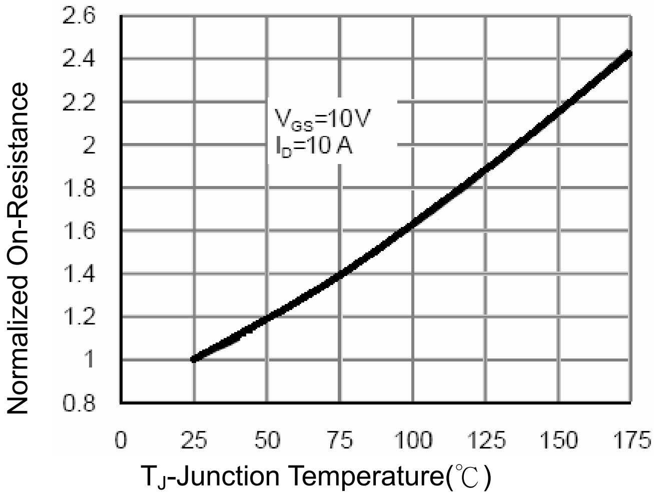



**Figure 4 Rdson-JunctionTemperature**

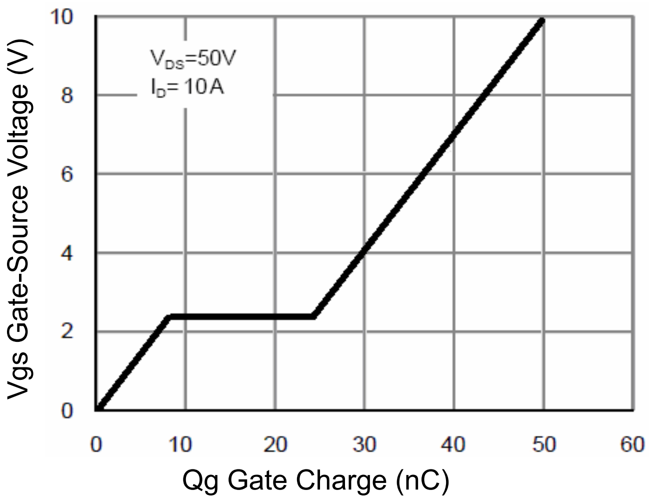



**Figure 5 Gate Charge**

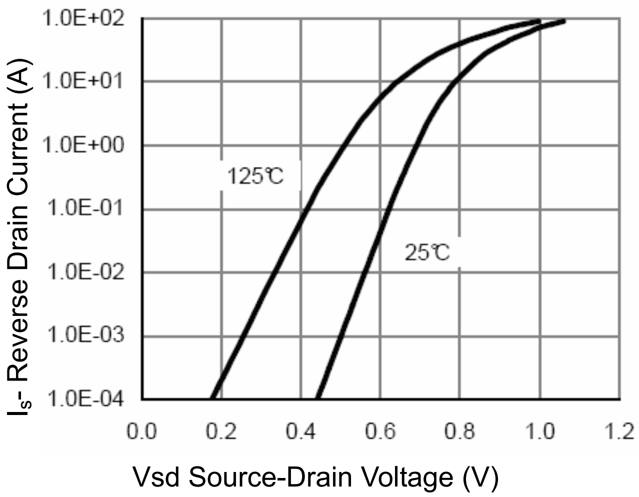



**Figure 6 Source- Drain Diode Forward**

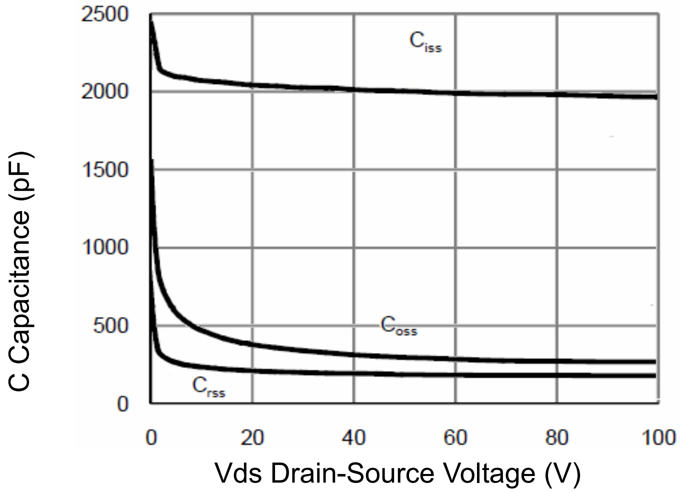



Figure 7 Capacitance vs Vds

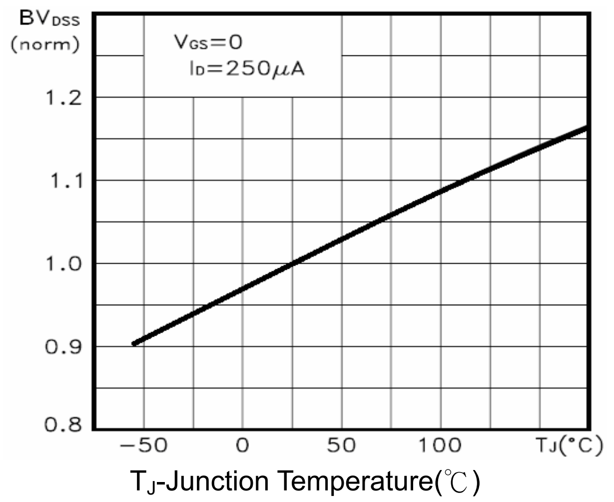



Figure 9 $BV_{DSS}$ vs Junction Temperature

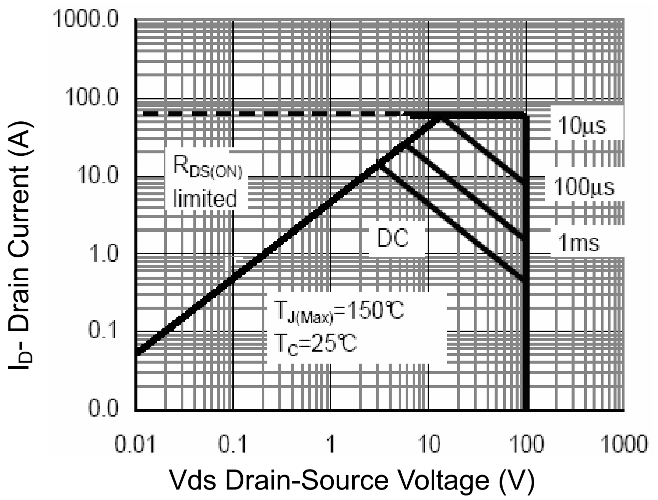



Figure 8 Safe Operation Area

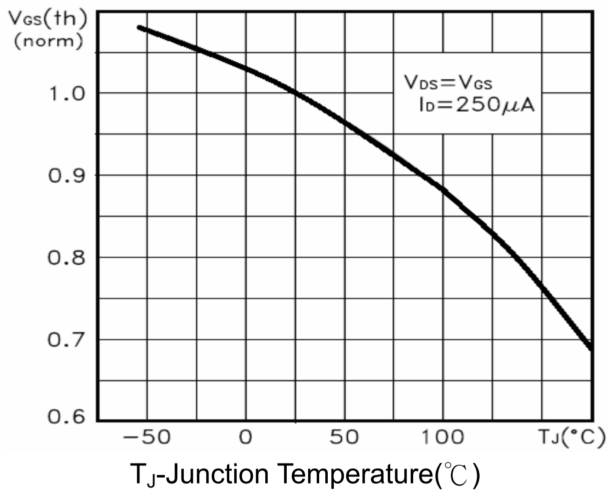



Figure 10 $V_{GS(th)}$ vs Junction Temperature

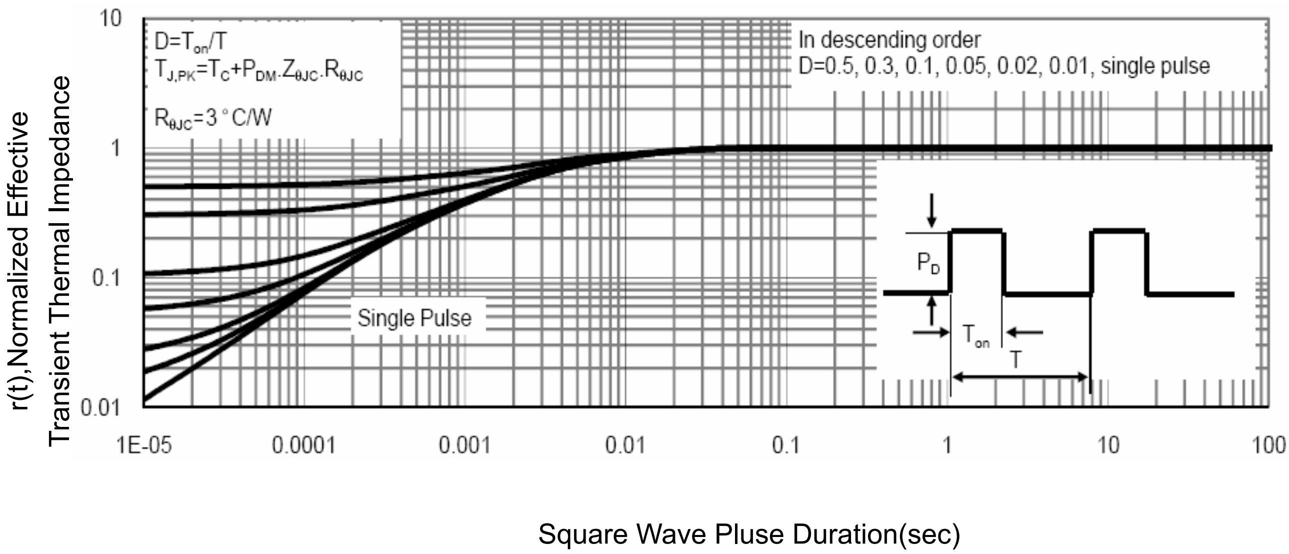
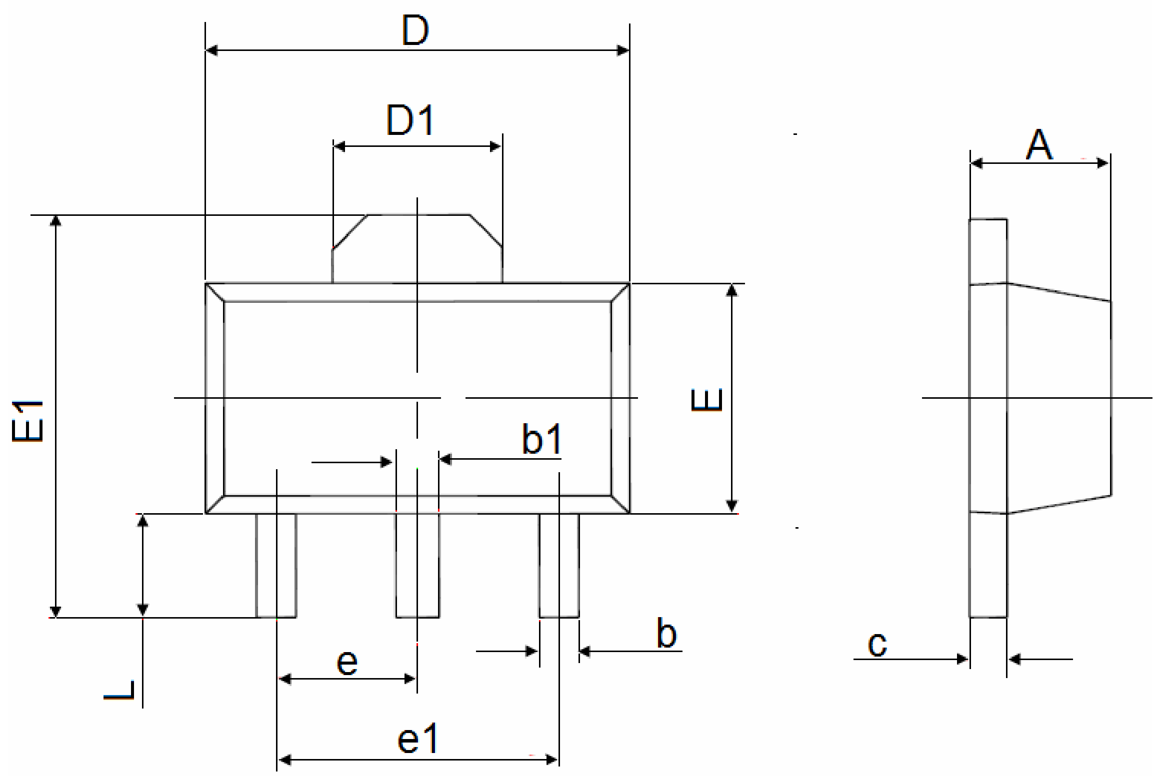



Figure 11 Normalized Maximum Transient Thermal Impedance

**SOT-89-3L Package Information**




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.400 | 1.600 | 0.055 | 0.063 |
| b | 0.320 | 0.520 | 0.013 | 0.020 |
| b1 | 0.400 | 0.580 | 0.016 | 0.023 |
| c | 0.350 | 0.440 | 0.014 | 0.017 |
| D | 4.400 | 4.600 | 0.173 | 0.181 |
| D1 | 1.550 REF. | | 0.061 REF. | |
| E | 2.300 | 2.600 | 0.091 | 0.102 |
| E1 | 3.940 | 4.250 | 0.155 | 0.167 |
| e | 1.500 TYP. | | 0.060 TYP. | |
| e1 | 3.000 TYP. | | 0.118 TYP. | |
| L | 0.900 | 1.200 | 0.035 | 0.047 |

Flow (wave) soldering (solder dipping)

| Product | Peak Temperature | Dipping Time |
|---|---|---|
| Pb device | 245℃±5℃ | 5sec±1sec |
| Pb-Free device | 260℃+0/-5℃ | 5sec±1sec |

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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