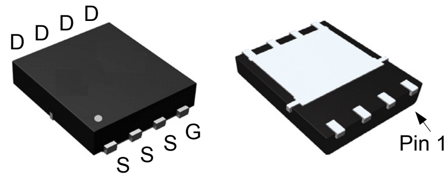
XPX200N06RD

60V N-Channel Enhancement Mode MOSFET

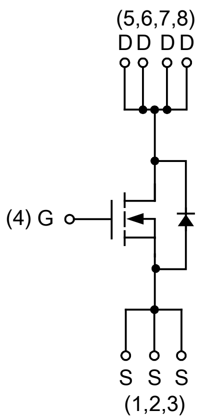
Description

The XPX200N06RD uses advanced technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 10V. This device is suitable for use as a Battery protection or in other Switching application.

Pin Description



DFN5x6A-8_EP



N-Channel MOSFET

General Features

V_{DS} = 60V I_D =200A

$R_{DS(ON)}$ < 1.6mΩ @ V_{GS}=10V

Application

Battery protection

Load switch

Uninterruptible power supply

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
XPX200N06RD	DFN5*6-8L	XPX200N06RD XXX YYYY	5000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Value	Unit
VDS	Drain source voltage	60	V
VGS	Gate source voltage	±20	V
I_D@T_A=25℃	Continuous drain current	200	A
I_D@T_A=70℃	Continuous drain current	110	A
IDM	Pulsed drain current	700	A
P_D@T_A=25℃	Power dissipation	114	W
EAS	Single pulsed avalanche energy	353	mJ
TSTG	Storage Temperature Range	-55 to 150	℃
Tj	Operation and storage temperature	-55 to 150	℃
RθJC	Thermal resistance, junction-case	1.1	°C/W
RθJA	Thermal resistance, junction-ambient5)	25	°C/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	60	71	-	V
IGSS	Gate-body Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
IDSS T_J=25°C	Zero Gate Voltage Drain Current	V_{DS} = 60V, V_{GS} = 0V	-	-	1	μA
IDSS T_J=100°C			-	-	100	
VGS(th)	Gate-Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	2.0	2.8	4.0	V
RDS(on)	Drain-Source On-Resistance[4]	V_{GS} = 10V, I_D = 20A	-	1.6	2.2	mΩ
gfs	Forward Transconductance[4]	V_{DS} = 10V, I_D = 20A	-	89	-	S
Ciss	Input Capacitance	V_{DS} = 30V, V_{GS} =0V, f =1MHz	-	4150	-	pF
Coss	Output Capacitance		-	1075	-	
Crss	Reverse Transfer Capacitance		-	33	-	
RG	Gate Resistance	f =1MHz	-	2.2	-	Ω
Q_g	Total Gate Charge	V_{GS} = 10V, V_{DS} = 30V, I_D= 20A	-	69	-	nC
Qgs	Gate-Source Charge		-	17.2	-	
Qgd	Gate-Drain Charge		-	21	-	
td(on)	Turn-on Delay Time	V_{GS} =10V, V_{DD} = 30V, R_G = 3Ω, I_D= 20A	-	17.5	-	ns
t_r	Rise Time		-	18.1	-	
td(off)	Turn-off Delay Time		-	42	-	
t_f	Fall Time		-	22	-	
trr	Body Diode Reverse Recovery Time	I_F=20A , dI/dt=100A/μs	-	57	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	67.9	-	nC
VSD	Diode Forward Voltage[4]	I_S = 20A, V_{GS} = 0V	-	-	1.2	V
IS	Continuous Source Current T_C=25°C		-	-	180	A

Note

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The EAS data shows Max. rating . The test condition is VDD=25V,VGS=10V,L=0.1mH,IAS=38A

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation

Typical Characteristics

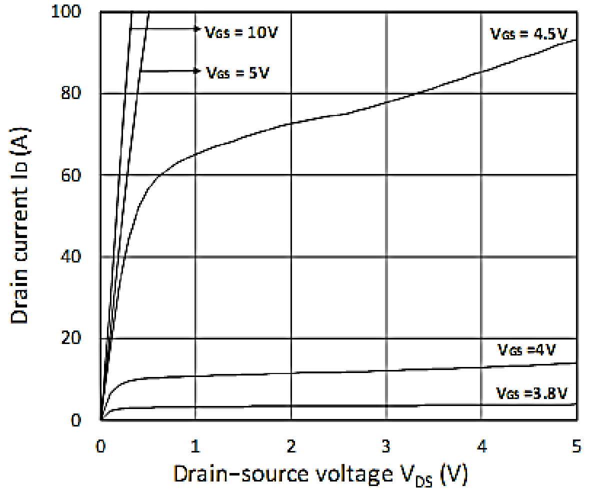


Figure 1. Output Characteristics

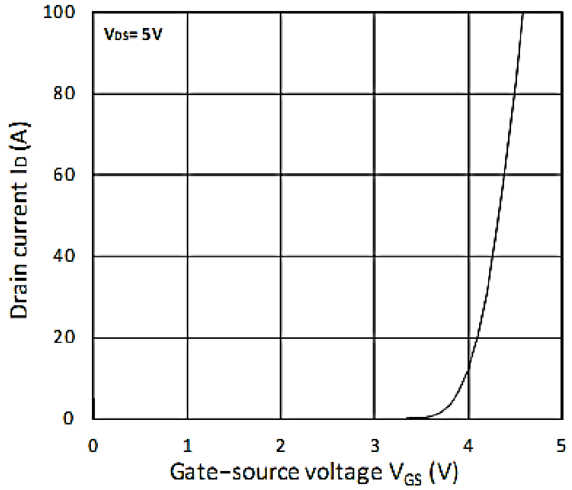


Figure 2. Transfer Characteristics

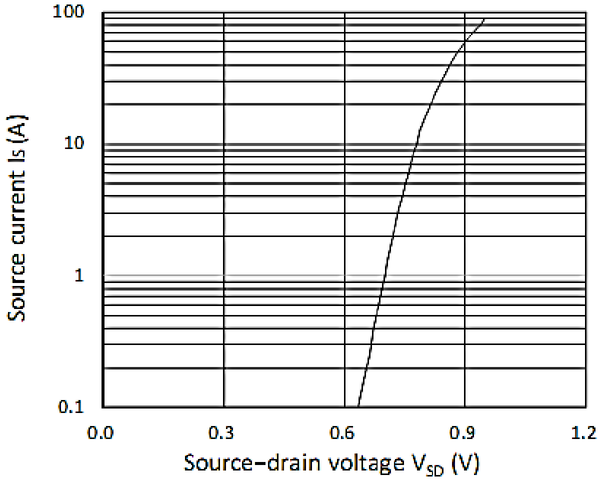


Figure 3. Forward Characteristics of Reverse

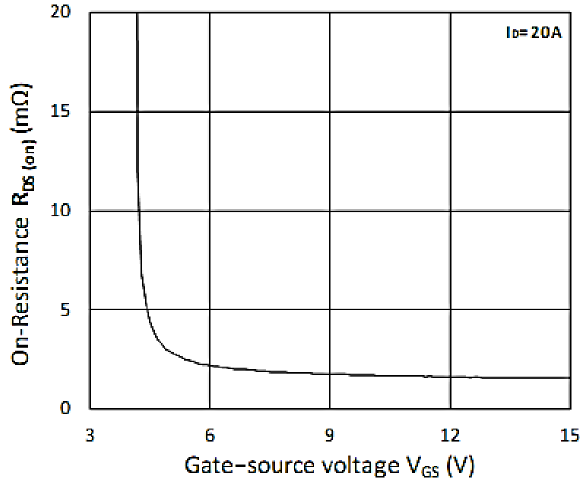


Figure 4. RDS(ON) vs.VGS

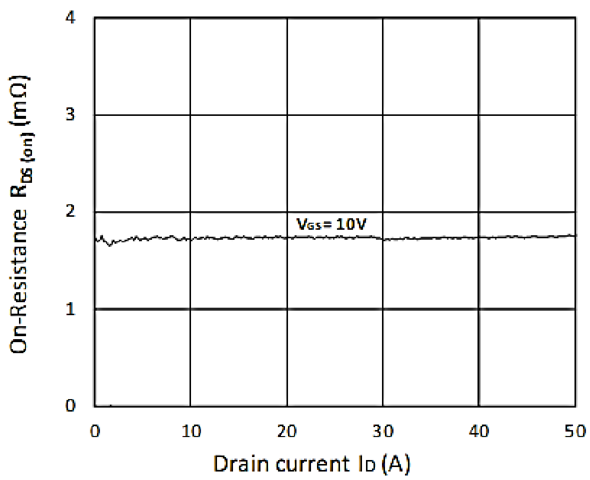


Figure 5. RDS(ON) vs. ID

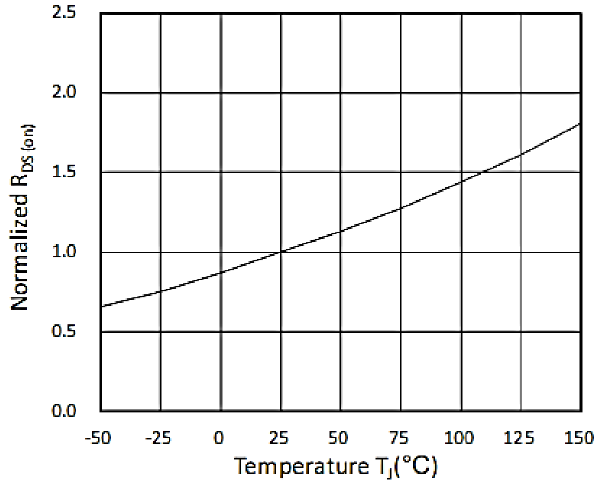


Figure 6. Normalized RDS(on) vs. Temperature

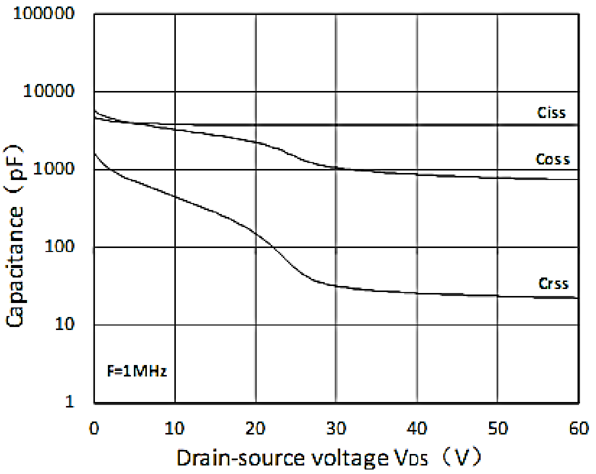


Figure 7. Capacitance Characteristics

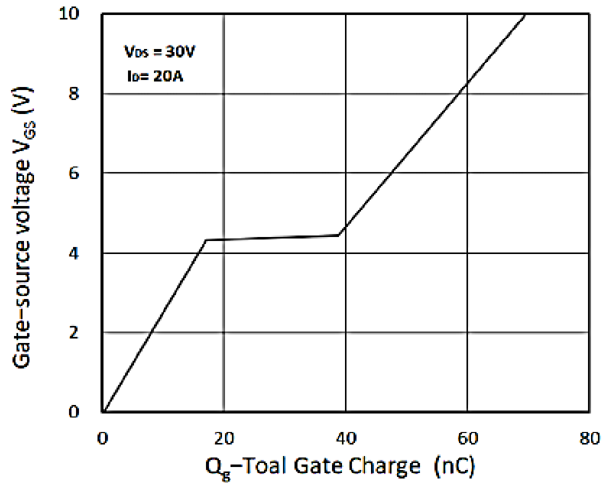


Figure 8. Gate Charge Characteristics

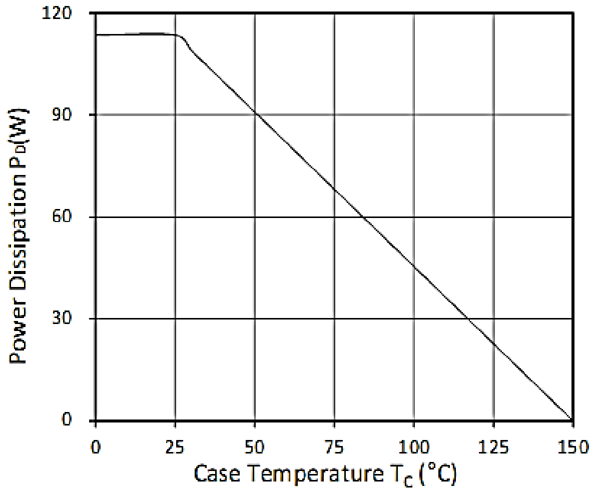


Figure 9. Power Dissipation

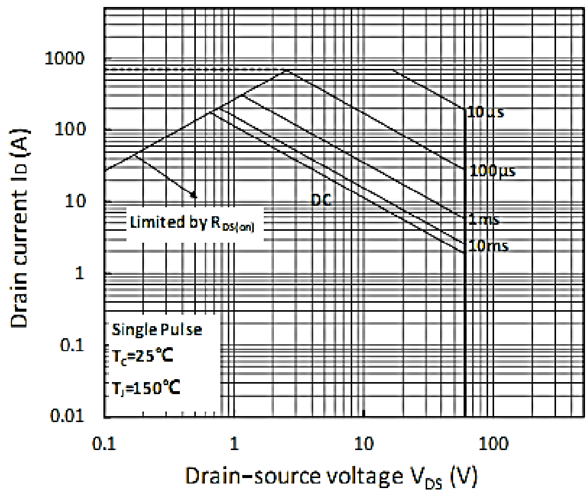


Figure10. Safe Operating Area

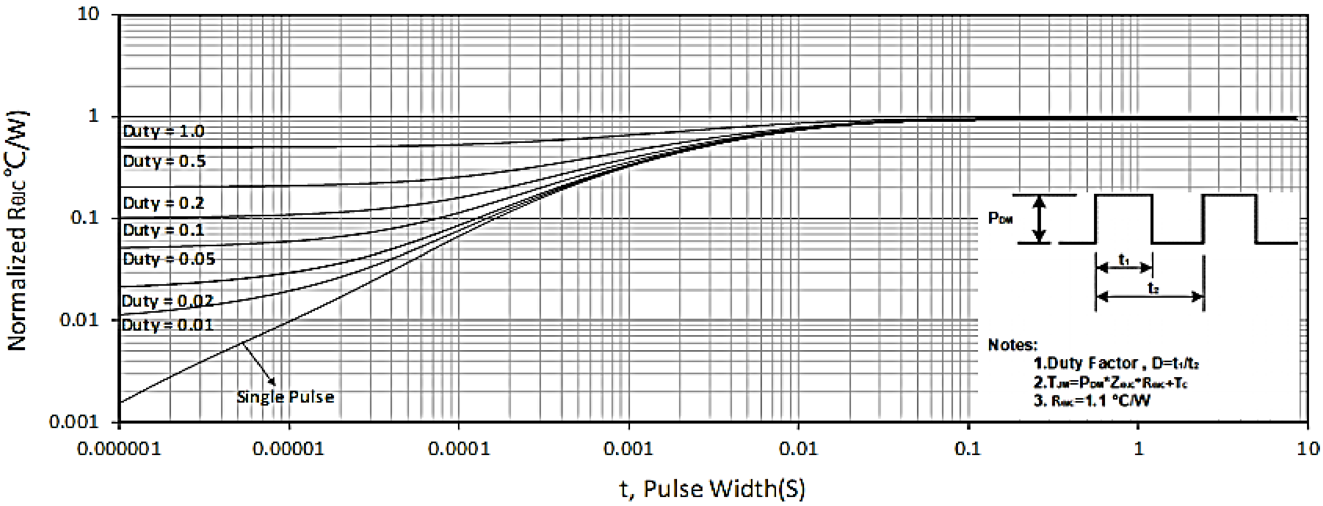
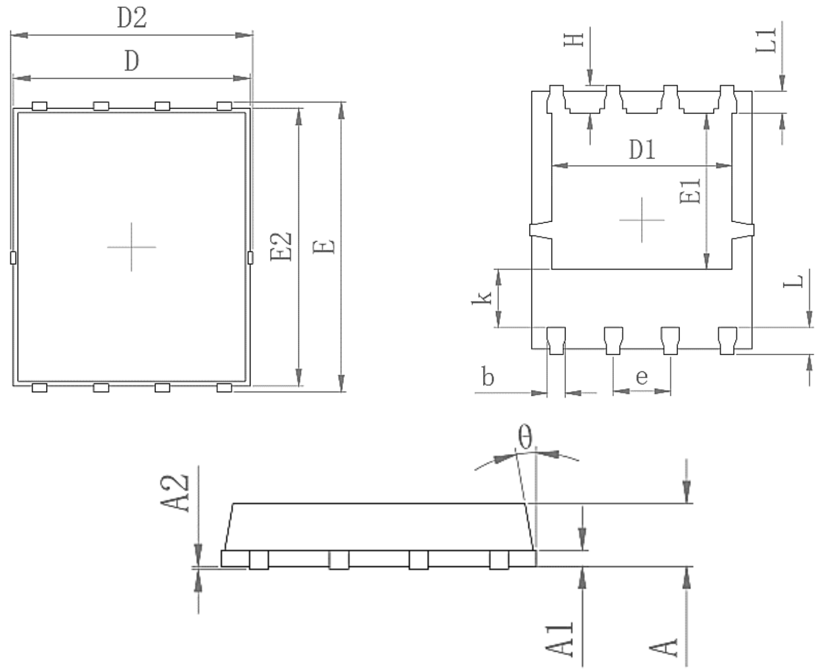


Figure 11. Normalized Maximum Transient Thermal Impedance

Package Mechanical Data-PDFN5X6-8L-XZT Single



Symbol	Common	
	mm	
	Mim	Max
A	0.90	1.10
A1	0.254 REF	
A2	0-0.05	
D	4.824	4.976
D1	3.910	4.110
D2	4.944	5.076
E	5.924	6.076
E1	3.375	3.575
E2	5.674	5.826
b	0.350	0.450
e	1.270	
L	0.534	0.686
L1	0.424	0.576
K	1.190	1.390
H	0.549	0.701
Φ	8°	12°

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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