-20V P-Channe Enhancement Mode MOSFET

RoHS COMPLIANT

Description

The XPX20L70RX uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

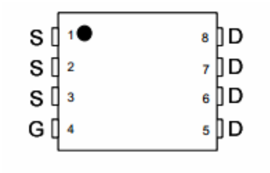
V_{DS} =-20V,I_D =-70A

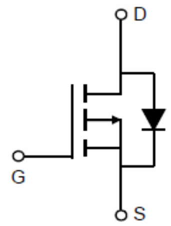
$R_{DS(ON)}$=6.5mΩ (typ) @ V_{GS}=-4.5V

$R_{DS(ON)}$=8mΩ (typ) @ V_{GS}=-2.5V

General Features

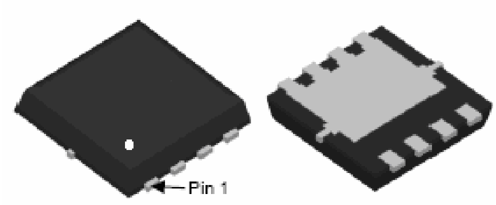
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation





Application

- Load switch
- Battery protection



DFN 3.3x3.3-8L

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
XPX20L70RX	XPX20L70RX	DFN 3.3x3.3-8L	-	-	5000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current-Continuous	I_D	-75	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	-45	A
Pulsed Drain Current	I_{DM}	-200	A
Maximum Power Dissipation	P_D	80	W
Single pulse avalanche energy (Note 5)	E_{AS}	180	mJ
Derating factor		0.64	W/℃
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃
Thermal Resistance,Junction-to-Case(Note 2)	$R_{θJC}$	1.6	℃/W

Electrical Characteristics (T_A= 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=-250μA	-20	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =-16V, V_{GS}=0V	-	-	-1	μA
		T_j=85°C	-	-	-5	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} =V_{GS}, I_{DS}=-250μA	-0.2	-0.6	-0.9	V
I_{GSS}	Gate Leakage Current	V_{GS}=±12V, V_{DS}=0V	-	-	±100	nA
$R_{DS(ON)}$	Drain-Source On-state Resistance [2]	V_{GS}=-4.5V, I_{DS}=-20A	-	6.5	8	mΩ
		V_{GS}=-2.5V, I_{DS}=-20A	-	8	11	
Body Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD}=-1A, V_{GS}=0V	-	-	-1.0	V
t_{rr}	Reverse Recovery Time	V_R=10V I_{DS}=20A, dI_{SD}/dt=100A/μs	-	78	-	ns
Qrr	Reverse Recovery Charge		-	495	-	nC
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS}=-15V V_{GS}=0V,f=1MHz	-	3013	-	pF
C_{oss}	Output Capacitance		-	427	-	
C_{rss}	Reverse transfer capacitance		-	316	-	
$t_{d(ON)}$	Turn-on delay Time	V_{DS}=-10V.V_{GS}=-4.5V, R_G=3Ω, I_D=-1A,R_L=0.5Ω	-	18	-	nS
t_r	Turn-on rise Time		-	52	-	
$t_{d(OFF)}$	Turn-off delay Time		-	285	-	
t_f	Turn-off rise Time		-	123	-	
Gate Charge Characteristics						
Q_g	Total Gate Charge	V_{DS} =-10V, V_{GS}=-4.5V I_{DS}=-20A	-	70	100	nC
Q_{gs}	Gate-Source Charge		-	9.2	-	
Q_{gd}	Gate-Drain Charge		-	18.4	-	

Note :
1.The data tested by surface mounted on a 1 $inch^2$ FR-4 board with 2OZ copper,t≦10sec.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is V_{DD}=-10V,V_{GS}=-10V,L=0.1mH,I_{AS}=-16A
4.The power dissipation is limited by 150℃ junction temperature
5.The Min. value is 100% EAS tested guarantee.
6.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

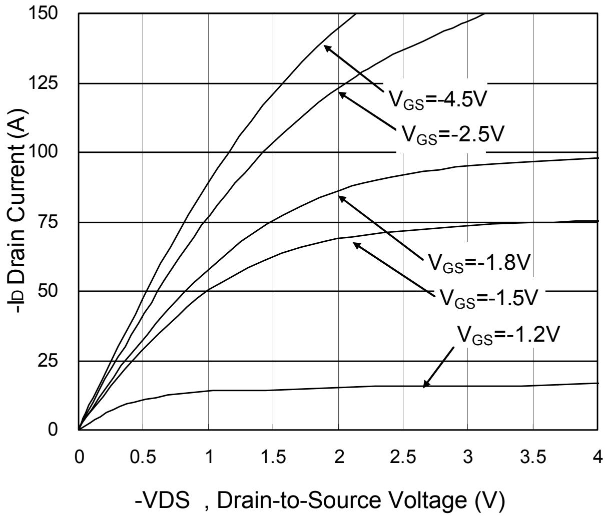


Fig.1 Typical Output Characteristics

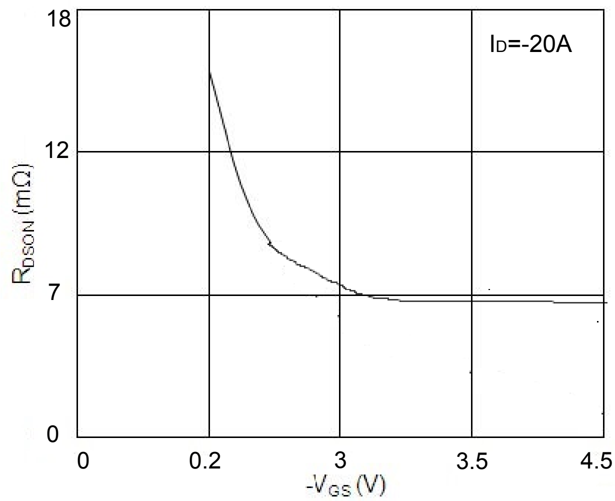


Fig.2 On-Resistance vs. G-S Voltage

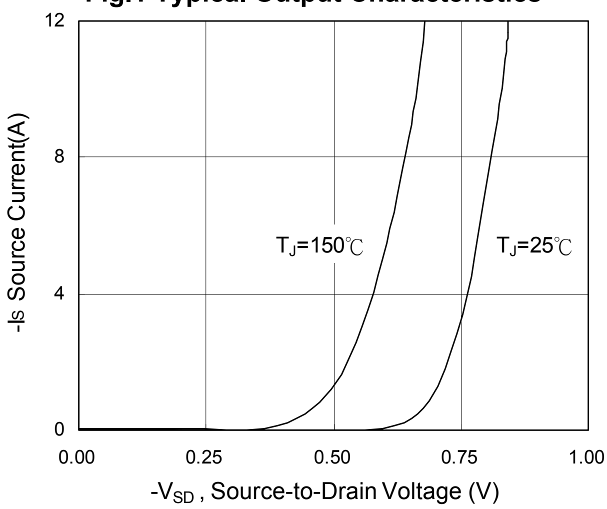


Fig.3 Forward Characteristics of Reverse

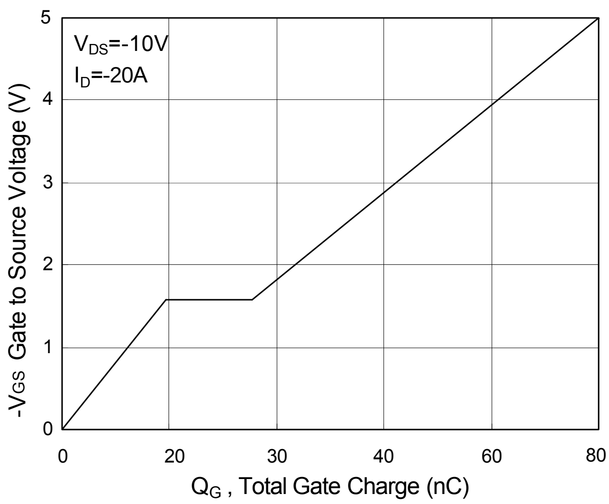


Fig.4 Gate-Charge Characteristics

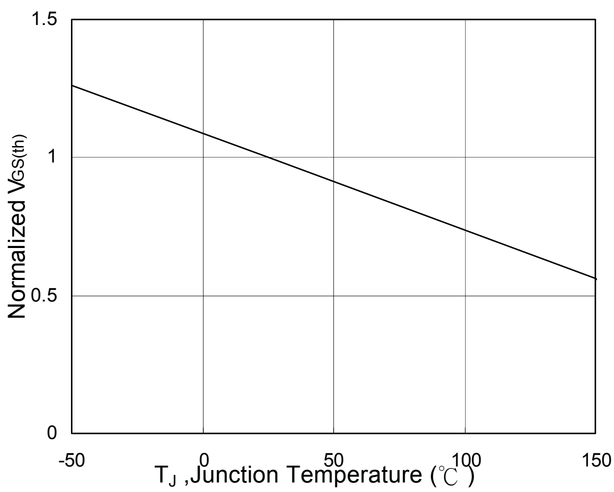


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

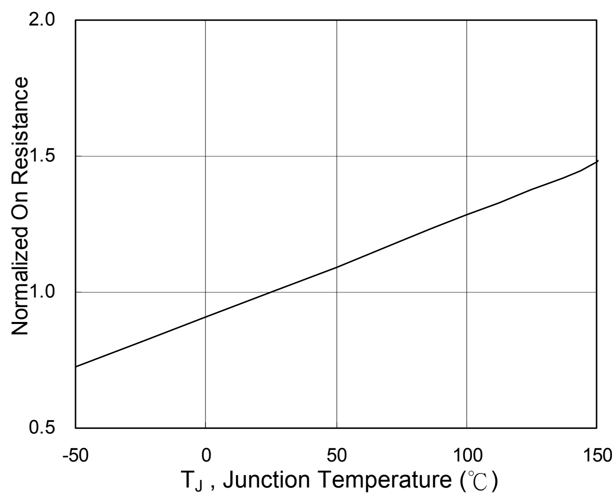


Fig.6 Normalized R_{DSON} vs. T_J

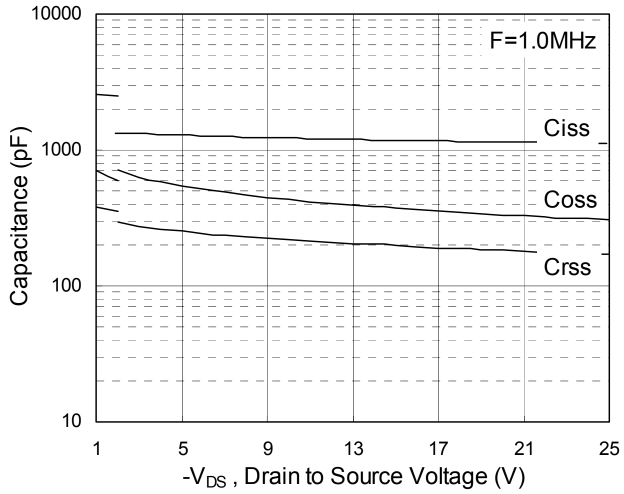


Fig.7 Capacitance

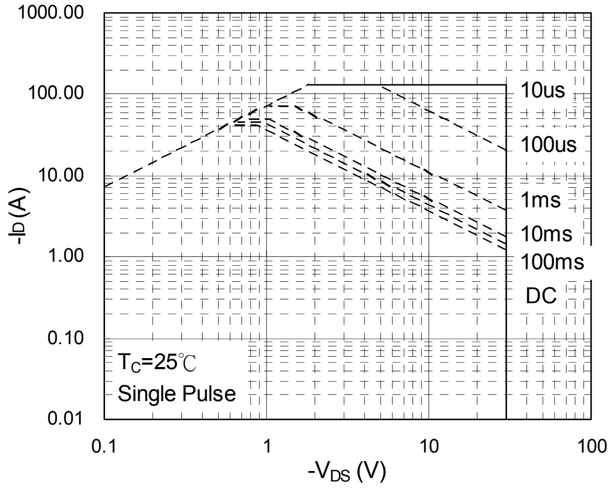


Fig.8 Safe Operating Area

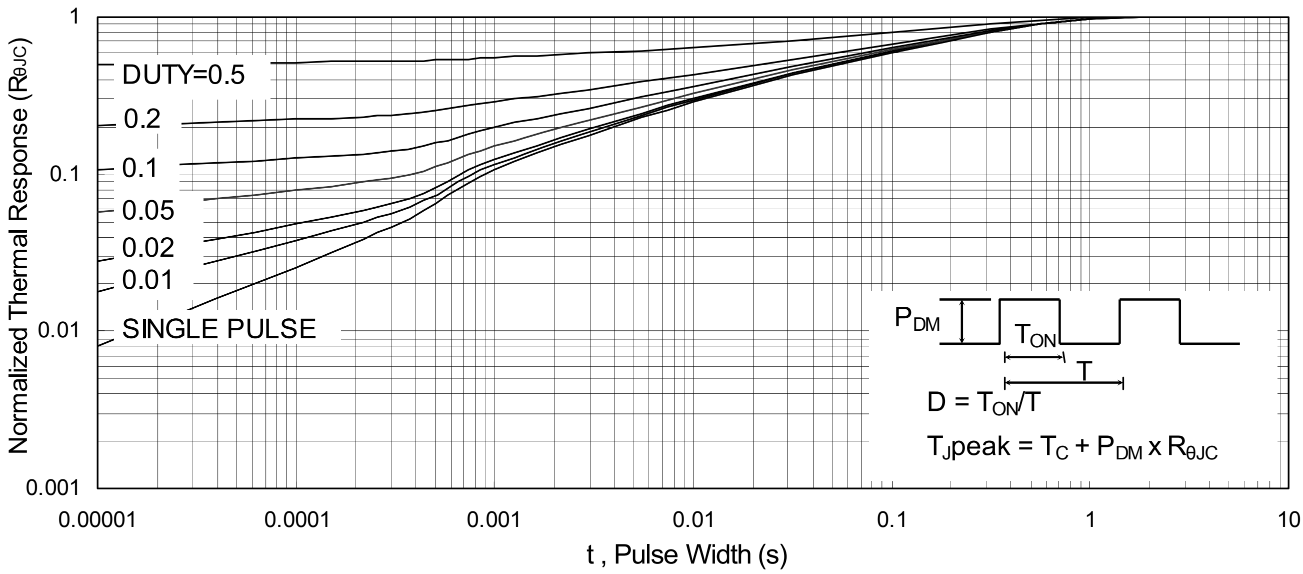
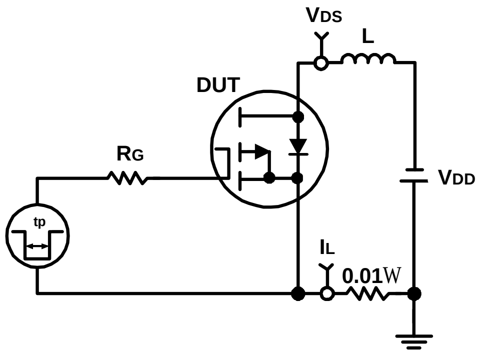
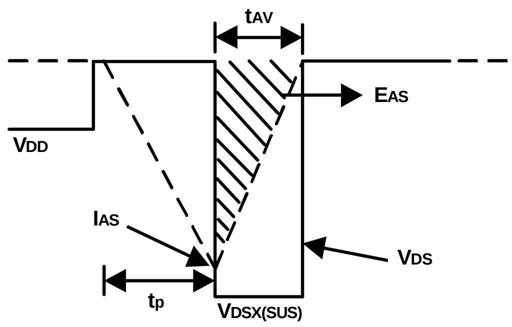


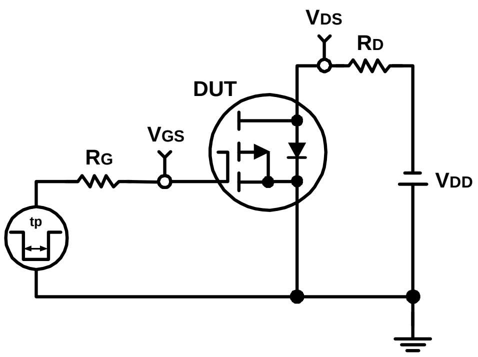
Fig.9 Normalized Maximum Transient Thermal Impedance

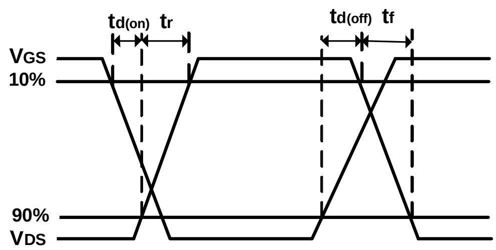
Avalanche Test Circuit and Waveforms





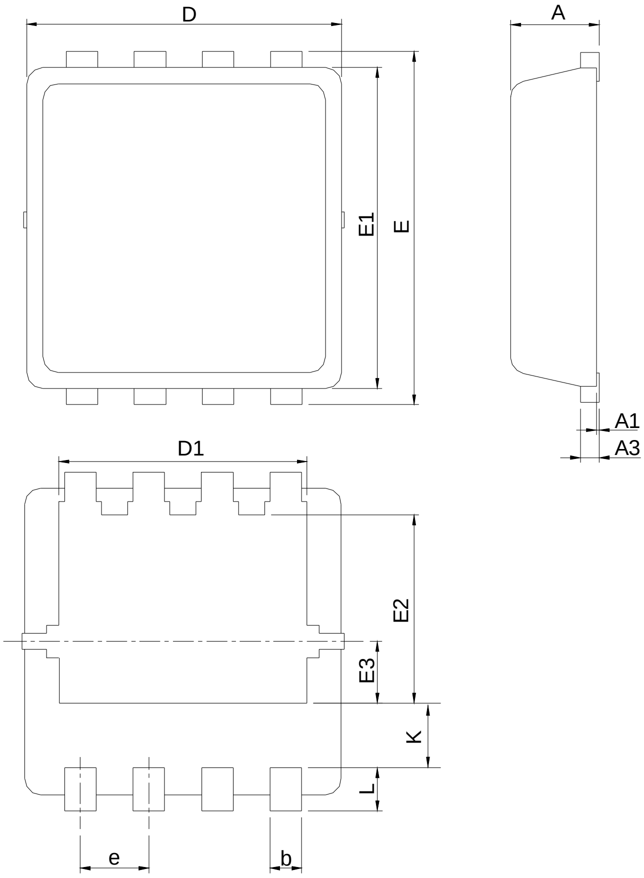
Switching Time Test Circuit and Waveforms





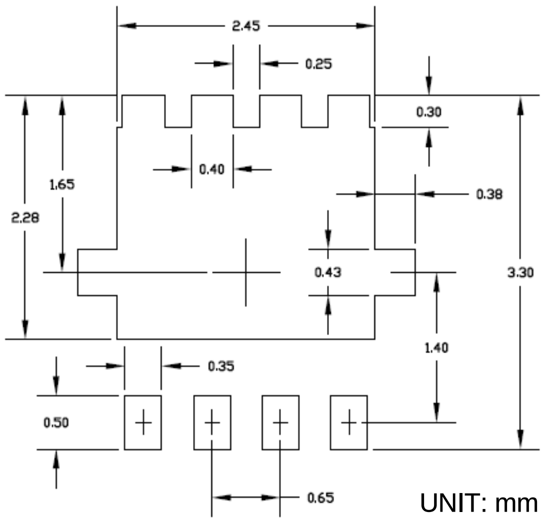
Package Information

DFN3x3-8



SYMBOL	DFN3x3-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.10	0.25	0.004	0.010
b	0.24	0.35	0.009	0.014
D	2.90	3.10	0.114	0.122
D1	2.25	2.45	0.089	0.096
E	3.10	3.30	0.122	0.130
E1	2.90	3.10	0.114	0.122
E2	1.65	1.85	0.065	0.073
E3	0.56	0.58	0.022	0.023
e	0.65 BSC		0.026 BSC	
K	0.475	0.775	0.019	0.031
L	0.30	0.50	0.012	0.020

RECOMMENDED LAND PATTERN



UNIT: mm

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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