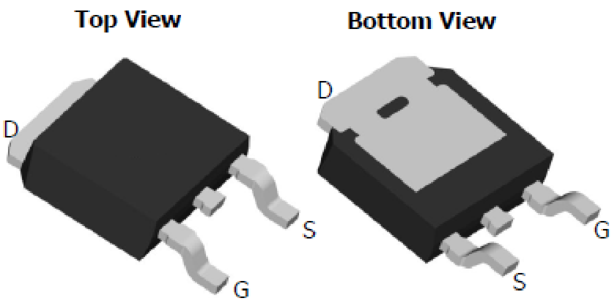
XPX2N120FD

200V N-Channel Enhancement Mode MOSFET

Description

The XPX2N12FD is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.



General Features

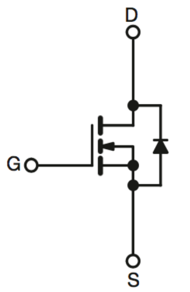
V_{DS} = 200V I_D =18A

$R_{DS(ON)}$ < 150mΩ @ V_{GS}=10V （**Type：120mΩ**）

Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



N-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
XPX2N120FD	TO-252-3L	XXX YYYY	2500

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Value	Unit
		TO-252	
VDSS	Drain-Source Voltage (V_{GS} = 0V)	200	V
ID	Continuous Drain Current	18	A
IDM	Pulsed Drain Current (note1)	72	A
VGS	Gate-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy (note2)	340	mJ
IAR	Avalanche Current (note1)	15	A
E_{AR}	Repetitive Avalanche Energy note1)	8.3	mJ
P_D	Power Dissipation (T_C = 25ºC)	104	W
TJ, Tstg	Operating Junction and Storage Temperature Range	-55~+150	ºC
RthJC	Thermal Resistance, Junction-to-Case	1.2	ºC/W
RthJA	Thermal Resistance, Junction-to-Ambient	62.5	ºC/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	200	220	--	V
IDSS	Zero Gate Voltage Drain Current	V_{DS} = 200V, V_{GS} = 0V, T_J = 25ºC	--	--	5	μA
		V_{DS} = 160V, V_{GS} = 0V, T_J = 125ºC	--	--	100	
IGSS	Gate-Source Leakage	V_{GS} = ±20V	--	--	±100	nA
VGS(th)	Gate-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1.0	1.6	3.0	V
RDS(on)	Drain-Source On-Resistance (Note3)	V_{GS} = 10V, I_D = 9A	--	120	150	mΩ
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz	--	1318	--	pF
C_{oss}	Output Capacitance		--	180	--	
C_{rss}	Reverse Transfer Capacitance		--	75	--	
Q_g	Total Gate Charge	V_{DD} = 160V, I_D = 18A, V_{GS} = 10V	--	41	--	nC
Q_{gs}	Gate-Source Charge		--	5.5	--	
Q_{gd}	Gate-Drain Charge		--	19.5	--	
td(on)	Turn-on Delay Time	V_{DD} = 100V, I_D = 18A, R_G = 25 Ω	--	24	--	ns
t_r	Turn-on Rise Time		--	45	--	
td(off)	Turn-off Delay Time		--	101	--	
t_f	Turn-off Fall Time		--	95	--	
I_S	Continuous Body Diode Current	T_C = 25 ºC	--	--	18	A
ISM	Pulsed Diode Forward Current		--	--	72	
V_{SD}	Body Diode Voltage	T_J = 25ºC, I_{SD} = 18A, V_{GS} = 0V	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V,I_S = 18A, di_F/dt =100A /μs	--	230	--	ns
Q_{rr}	Reverse Recovery Charge		--	1.8	--	μC

Note :

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The EAS data shows Max. rating . IAS = 15A, VDD = 50V, RG = 25 Ω, Starting TJ = 25 ºC

3、The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

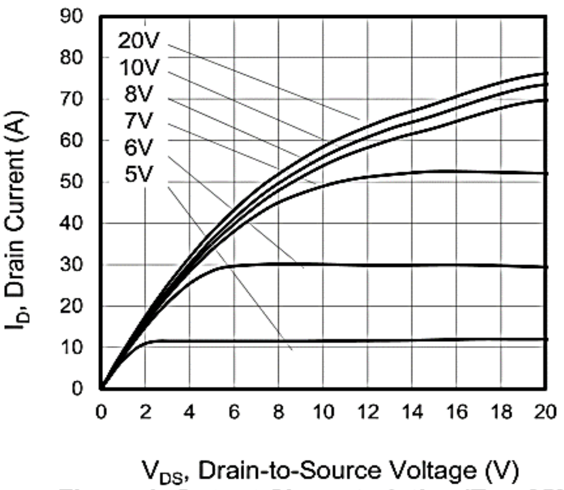


Figure 1. Output Characteristics (T_J = 25ºC)

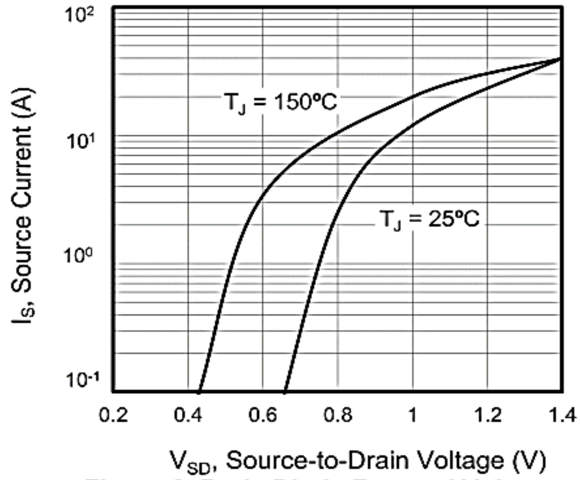


Figure 2. Body Diode Forward Voltage

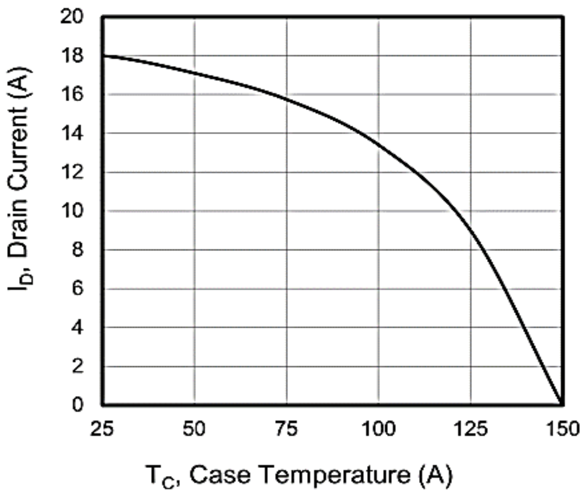


Figure 3. Drain Current vs. Temperature

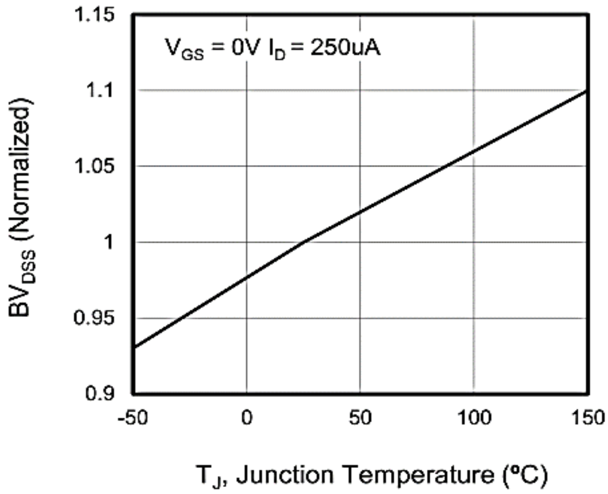


Figure 4. BV_{DSS} Variation vs. Temperature

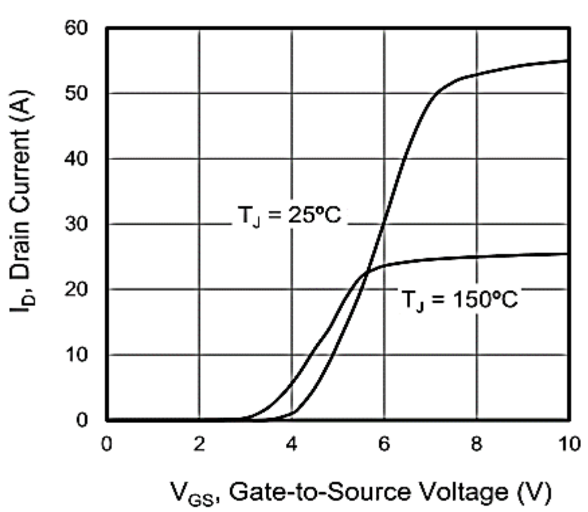


Figure 5. Transfer Characteristics

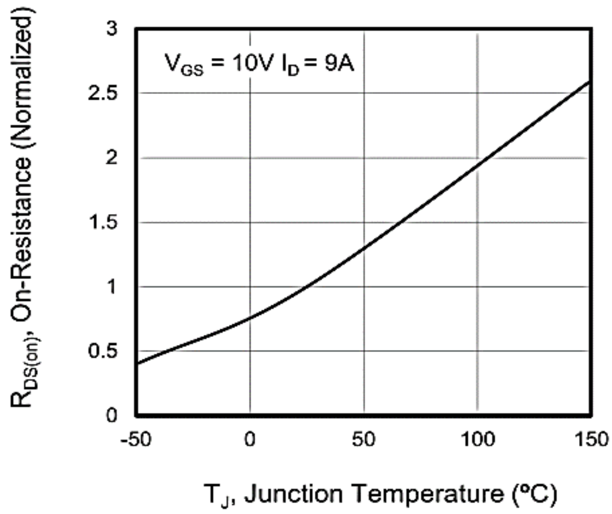


Figure 6. On-Resistance vs. Temperature

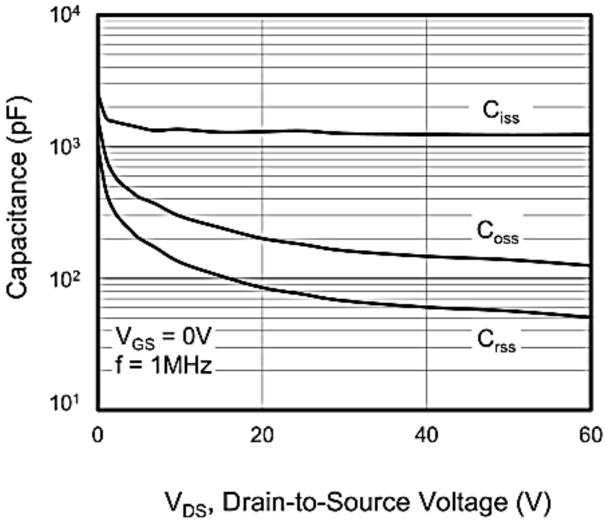


Figure 7. Capacitance

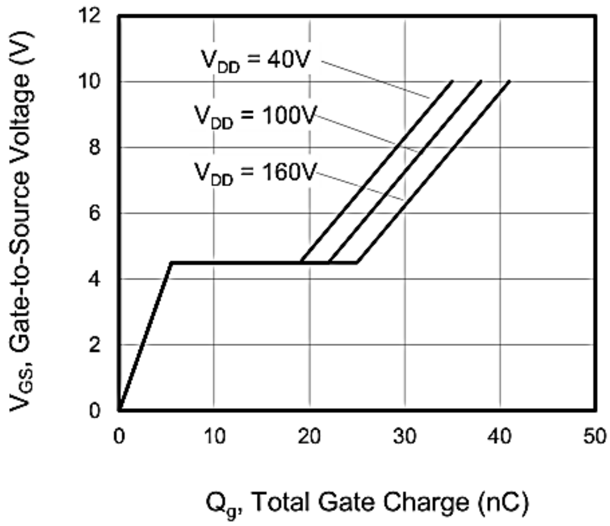


Figure 8. Gate Charge

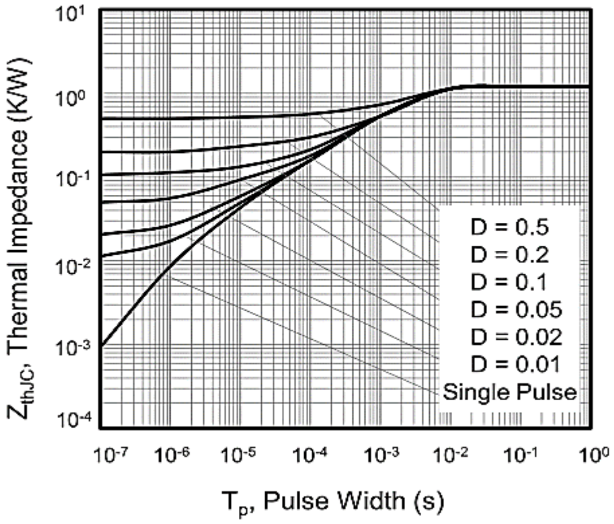


Figure 10. Transient Thermal Impedance

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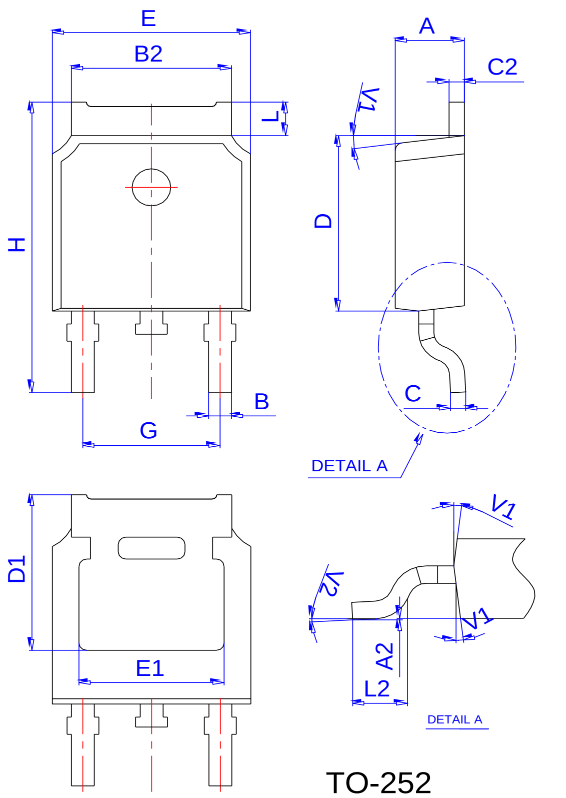
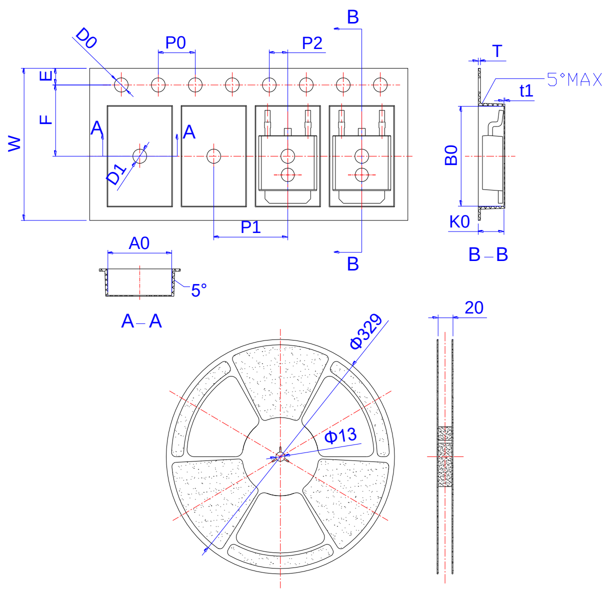
Package Mechanical Data：TO-252-3L



TO-252

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1		5.30REF			0.209REF	
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Reel Spectification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60			
P0	3.90	4.00	4.10			
P1	7.90	8.00	8.10			
P2	1.90	2.00	2.10			
A0	6.85	6.90	7.00			
B0	10.45	10.50	10.60			
K0	2.68	2.78	2.88			
T	0.24		0.27			
t1	0.10					
10P0	39.80	40.00	40.20			

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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