



Description

The XPX3080SFD uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

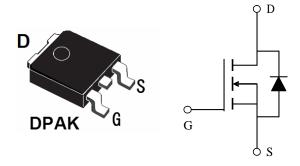
General Features

- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

 $V_{DS} = 30V, I_{D} = 80A$ $R_{DS}(ON) = 4.7 m\Omega \text{ (typ)} @ V_{GS} = 10V$ $R_{DS}(ON) = 6.0 m\Omega \text{ (typ)} @ V_{GS} = 4.5V$



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
3080S	XPX3080SFD	TO-252-2L	-	-	-

Absolute Maximum Ratings (T_C=25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	VDS	30	V
Gate-Source Voltage	Vgs	±20	V
Drain Current-Continuous	I _D	80	Α
Drain Current-Continuous(T _C =100 °C)	I _D (100℃)	50	Α
Pulsed Drain Current	I _{DM}	180	Α
Maximum Power Dissipation	P _D	83	W
Derating factor		0.56	W/℃
Single pulse avalanche energy (Note 5)	E _{AS}	306	mJ
Operating Junction and Storage Temperature Range	T_{J}, T_{STG}	-55 To 175	$^{\circ}$ C
Thermal Resistance,Junction-to-Case ^(Note 2)	R _{eJC}	1.8	°C/W



Electrical Characteristics (T_C=25 °C unless otherwise noted)

Parameter	Symbol	Condition	n Min		Max	Unit	
Off Characteristics	<u>.</u>						
Drain-Source Breakdown Voltage BV _{DSS}		V _{GS} =0V I _D =250μA	30	-	-	V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V,V _{GS} =0V	-	-	1	μΑ	
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA	
On Characteristics (Note 3)	<u>.</u>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_{D}=250\mu A$	1	1.6	2.5	V	
Drain Course On State Besistance	_	V _{GS} =10V, I _D =30A	-	4.7	6.5	mΩ	
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =5V, I _D =25A	-	6.0	8.0		
Forward Transconductance	g Fs	V _{DS} =5V,I _D =25A	20	-	-	S	
Dynamic Characteristics (Note4)	<u> </u>		•				
Input Capacitance	C _{lss}	\/ -45\/\/ -0\/	-	1486	-	PF	
Output Capacitance	C _{oss}	V_{DS} =15V, V_{GS} =0V, F=1.0MHz	-	260	-	PF	
Reverse Transfer Capacitance	C _{rss}	F=1.UIVIDZ	-	242	-	PF	
Switching Characteristics (Note 4)	<u>.</u>						
Turn-on Delay Time	t _{d(on)}		-	20	-	nS	
Turn-on Rise Time	t _r	V _{DD} =10V,I _D =30A	-	15	-	nS	
Turn-Off Delay Time	t _{d(off)}	V_{GS} =10 V , R_{GEN} =2.7 Ω	-	60	-	nS	
Turn-Off Fall Time	t _f		-	10	-	nS	
Total Gate Charge	Qg	\/ -40\/ L -20A	-	60.5	-	nC	
Gate-Source Charge	Q _{gs}	V_{DS} =10V, I_{D} =30A, V_{GS} =10V	-	8.1	-	nC	
Gate-Drain Charge	Q _{gd}	V _{GS} =10V	-	7.8	-	nC	
Drain-Source Diode Characteristics	<u>.</u>						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =24A	-	-	1.2	V	
Diode Forward Current (Note 2)	Is		-	-	80	Α	
Reverse Recovery Time	t _{rr}	TJ = 25°C, IF = 80A	-	32	50	nS	
Reverse Recovery Charge	Qrr	$di/dt = 100A/\mu s^{(Note3)}$	-	12	20	nC	
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD				y LS+LD)	

Notes

- $\textbf{1.} \ \ \textbf{Repetitive Rating: Pulse width limited by maximum junction temperature.}$
- **2.** Surface Mounted on FR4 Board, $t \le 10$ sec.
- 3. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.
- 4. Guaranteed by design, not subject to production
- **5.** EAS condition: Tj=25 $^{\circ}$ C,VDD=15V,VG=10V,L=0.5mH,Rg=25 Ω , IAS=35A



Typical Electrical and Thermal Characteristics (Curves)

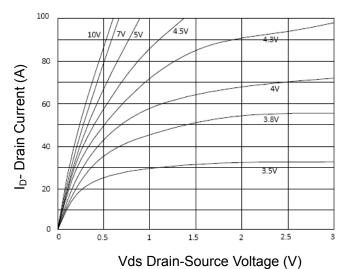


Figure 1 Output Characteristics

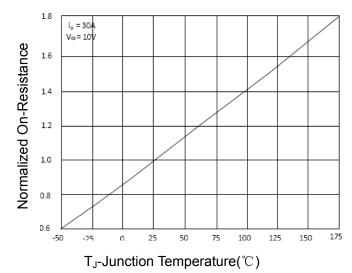
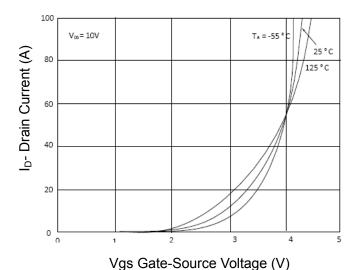


Figure 4 Rdson-JunctionTemperature



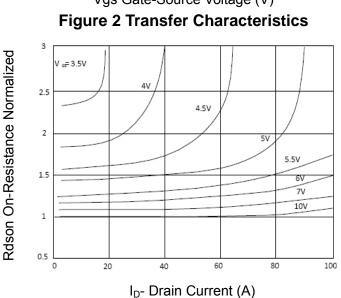
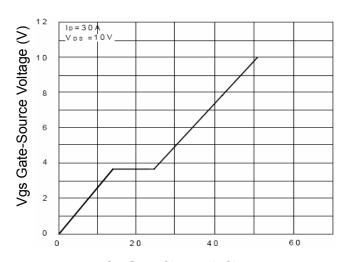


Figure 3 Rdson- Drain Current



Qg Gate Charge (nC)
Figure 5 Gate Charge

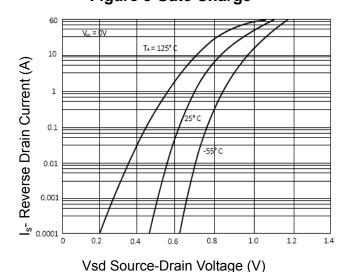
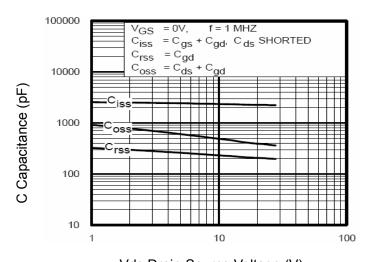
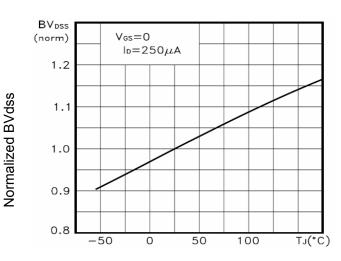


Figure 6 Source- Drain Diode Forward





Vds Drain-Source Voltage (V)



 T_{J} -Junction Temperature(${}^{\circ}\mathbb{C}$)

Figure 9 BV_{DSS} vs Junction Temperature



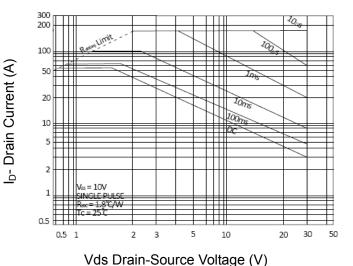
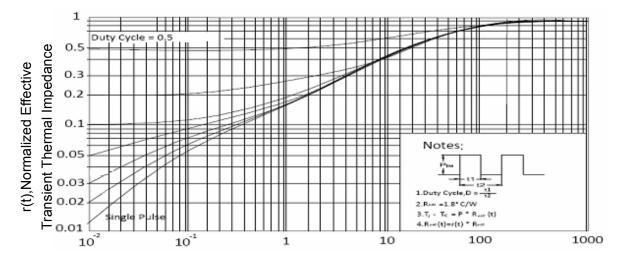


Figure 8 Safe Operation Area

V_{GS}(th) (norm)
1.0
0.9
0.8
0.7
0.6
-50
0
50
100
TJ(°C)

 T_J -Junction Temperature($^{\circ}$ C)

Figure 10 V_{GS(th)} vs Junction Temperature

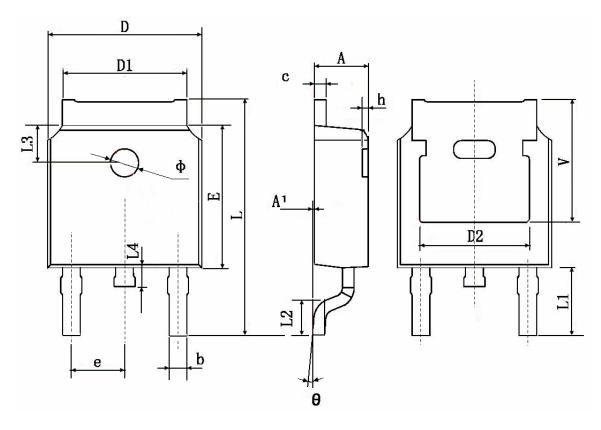


Square Wave Pluse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance



TO-252 Package Information



Ol	Dimensions	In Millimeters	Dimensions In Inches		
Symbol	Min.	Max.	Min.	Max.	
А	2.200	2.400	0.087	0.094	
A1	0.000	0.127	0.000	0.005	
b	0.660	0.860	0.026	0.034	
С	0.460	0.580	0.018	0.023	
D	6.500	6.700	0.256	0.264	
D1	5.100	5.460	0.201	0.215	
D2	4.830 TYP.		0.190 TYP.		
E	6.000	6.200	0.236	0.244	
е	2.186	2.386	0.086	0.094	
L	9.800	10.400	0.386	0.409	
L1	2.900 TYP.		0.114 TYP.		
L2	1.400	1.700	0.055	0.067	
L3	1.600 TYP.		0.063 TYP.		
L4	0.600	1.000	0.024	0.039	
Ф	1.100	1.300	0.043	0.051	
θ	0°	8°	0°	8°	
h	0.000	0.300	0.000	0.012	
V	5.350 TYP.		0.211	TYP.	



Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃ 5sec±1sec	
Pb-Free device	260℃+0/-5℃	5sec±1sec



This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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