

**Description**

The XPX320N15LL uses advanced technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 10V. This device is suitable for use as a Battery protection or in other Switching application.

**General Features**

$V_{DS} = 150V$   $I_D = 320A$

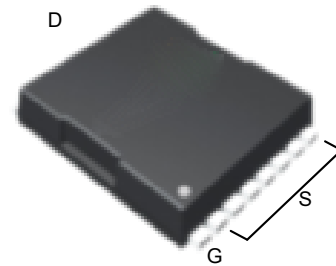
$R_{DS(ON)} < 3.2m\Omega @ V_{GS}=10V$

**Application**

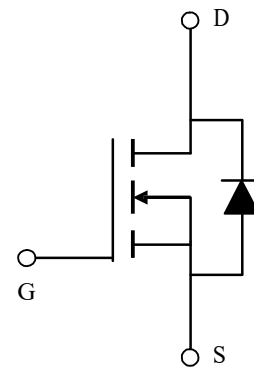
DC/DC Converter

LED Backlighting

Power Management Switches



TOLL


**Package Marking and Ordering Information**

Product ID	Pack	Marking	Qty(PCS)
XPX320N15LL	TOLLA-8L	XPX320N15LL XXX YYYY	2000

**Absolute Maximum Ratings ( $T_C=25^\circ C$  unless otherwise noted)**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	150	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	320	A
$I_D @ T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	188	A
IDM	Pulsed Drain Current	817	A
EAS	Single Pulse Avalanche Energy	2201	mJ
IAS	Avalanche Current	88	A
$P_D @ T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	600	W
TSTG	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	0.25	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case	40	$^\circ C/W$

**Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V I <sub>D</sub> = 250μA	150	165		V
IDSS	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 150V, V <sub>GS</sub> = 0V			1.0	nA
IDSS T <sub>J</sub> = 55°C	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 150V, T <sub>J</sub> = 55°C			5.0	
IGSS	Gate-Body Leakage Current	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V			±100	nA
VGS(th)	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2.5	3.2	4.5	V
RDS(ON)	Static Drain-Source	V <sub>GS</sub> = 10V, I <sub>D</sub> =40A		3.3	4.2	mΩ
gFS	Forward Transconductance	V <sub>DS</sub> = 5V, I <sub>D</sub> = 20A		65		S
R <sub>g</sub>	Gate Resistance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V, f = 1MHz		2.4		Ω
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1MHz		6550		pF
C <sub>oss</sub>	Output Capacitance			772		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			6.7		pF
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 to 10V V <sub>DS</sub> = 75V, I <sub>D</sub> = 20A		88		nC
Q <sub>gs</sub>	Gate Source Charge			32		nC
Q <sub>gd</sub>	Gate Drain Charge			16		nC
tD(on)	Turn-On DelayTime	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 75V R <sub>L</sub> = 3.75 Ω , R <sub>GEN</sub> = 6Ω		48		ns
t <sub>r</sub>	Turn-On Rise Time			90		ns
tD(off)	Turn-Off DelayTime			94		ns
t <sub>f</sub>	Turn-Off Fall Time			60		ns
trr	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, dI/dt=500A/μs		122		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=500A/μs		279		nC
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> = 1A, V <sub>GS</sub> = 0V		0.71	1.0	V
I <sub>S</sub>	Diode Continuous Current	T <sub>C</sub> = 25°C			600	A

**Notes:**

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
3. The EAS data shows Max. rating . The test condition is V<sub>DD</sub>=50V, V<sub>GS</sub>=10V, L=0.1mH, I<sub>AS</sub>=88A
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.

**Typical Characteristics**

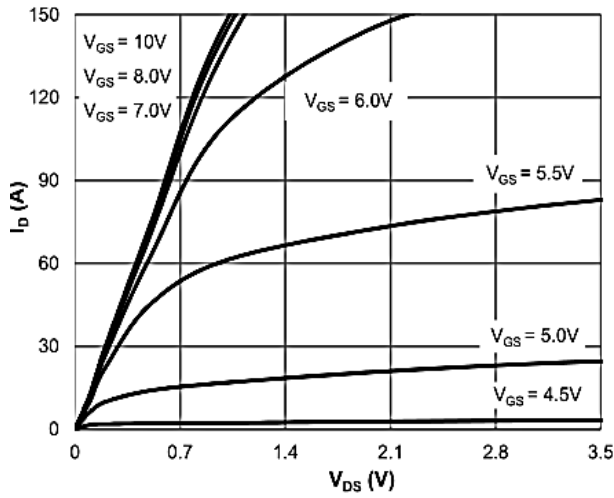


Figure 1: Saturation Characteristics

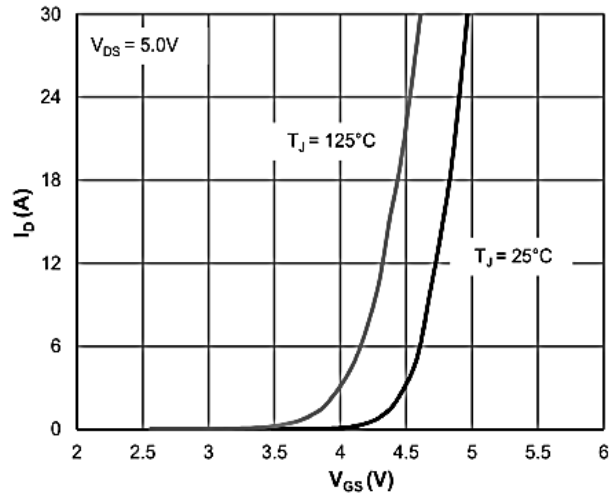


Figure 2: Transfer Characteristics

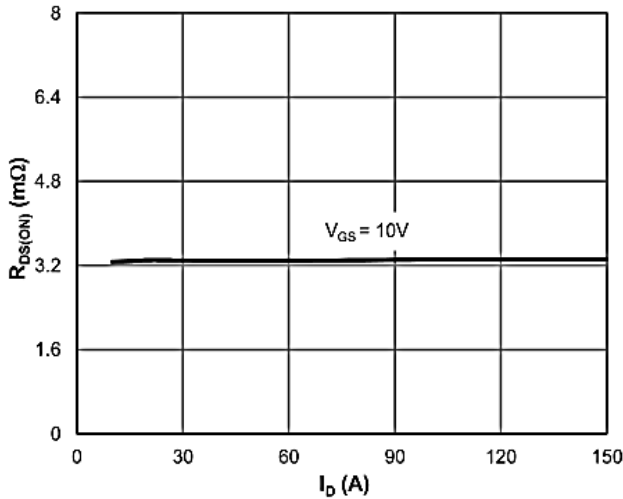


Figure 3: R\_DS(ON) vs. Drain Current

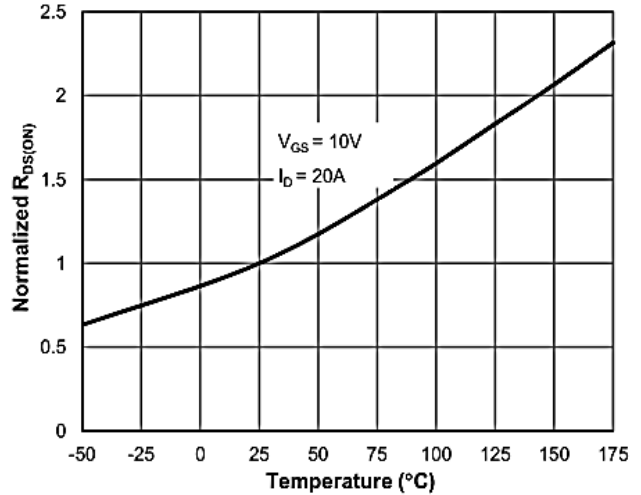


Figure 4: R\_DS(ON) vs. Junction Temperature

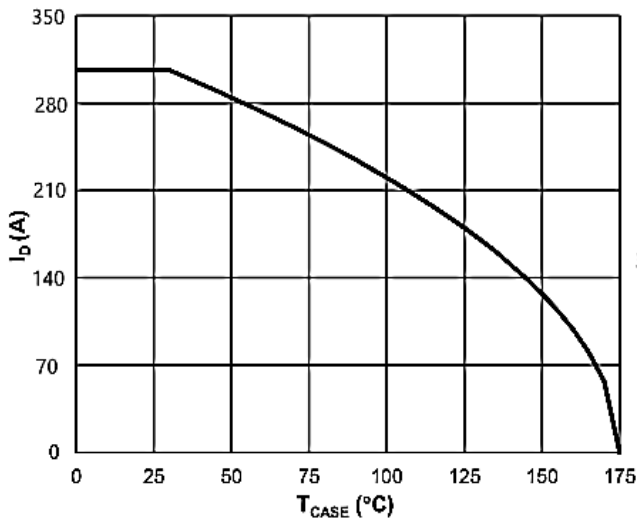


Figure 5: Current De-rating

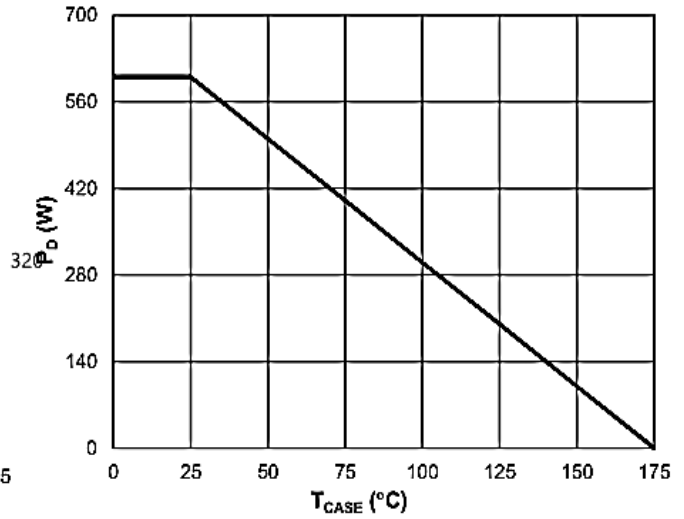


Figure 6: Power De-rating

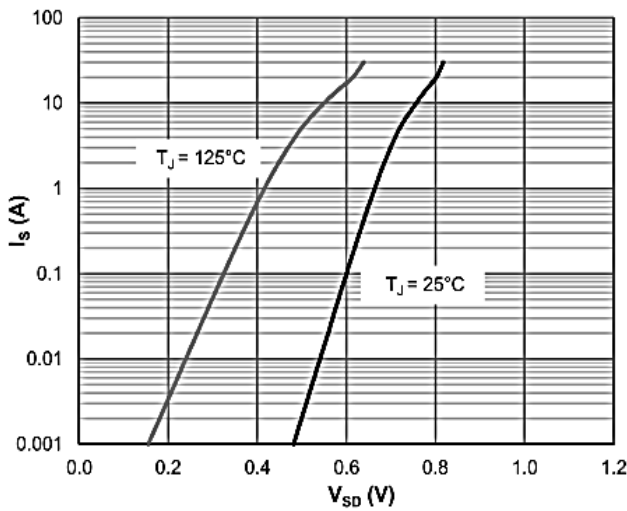


Figure 7: Body-Diode Characteristics

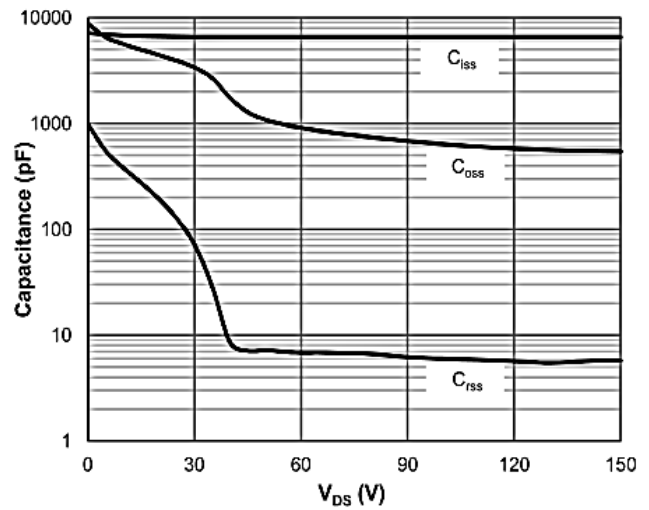


Figure 8: Capacitance Characteristics

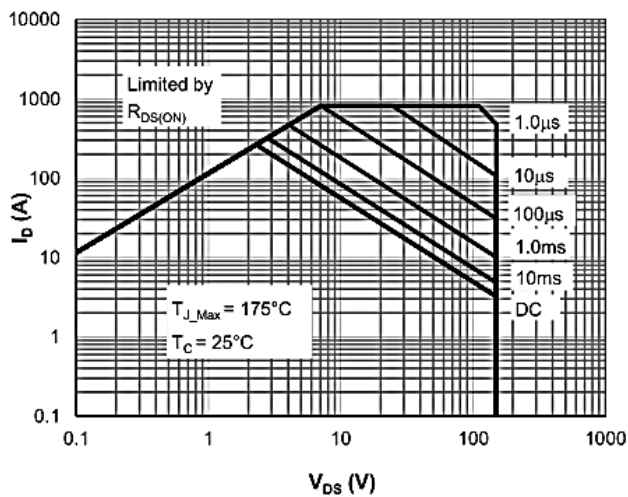


Figure 9: Maximum Safe Operating Area

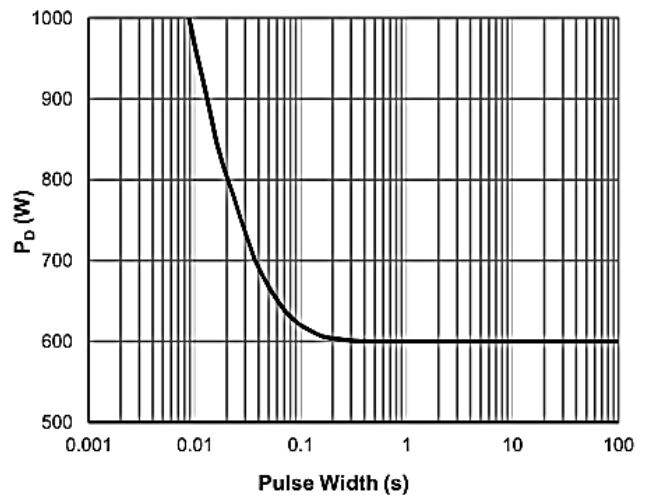
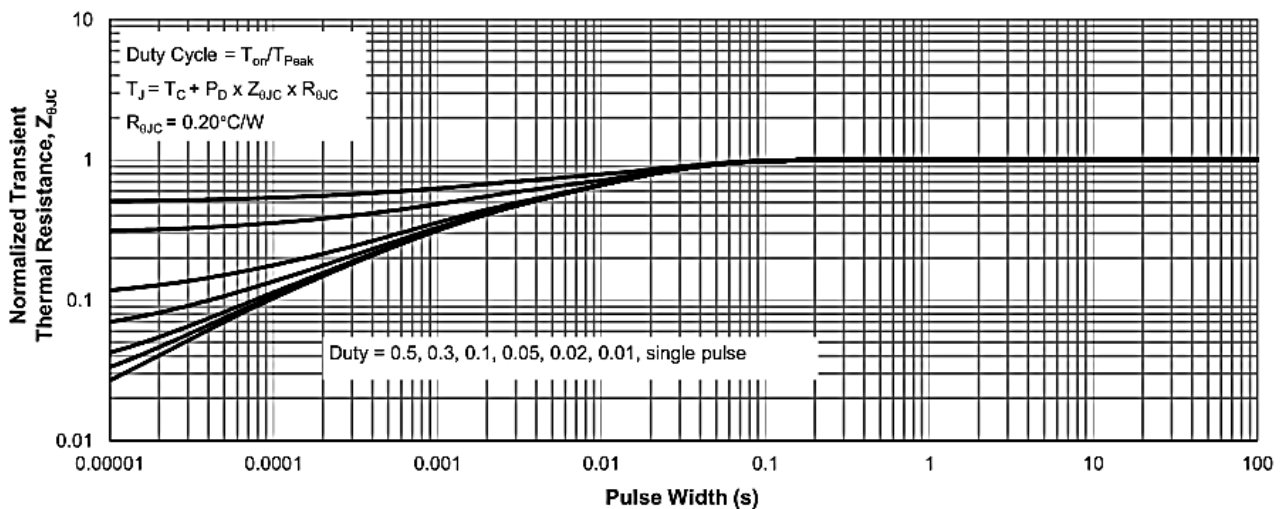
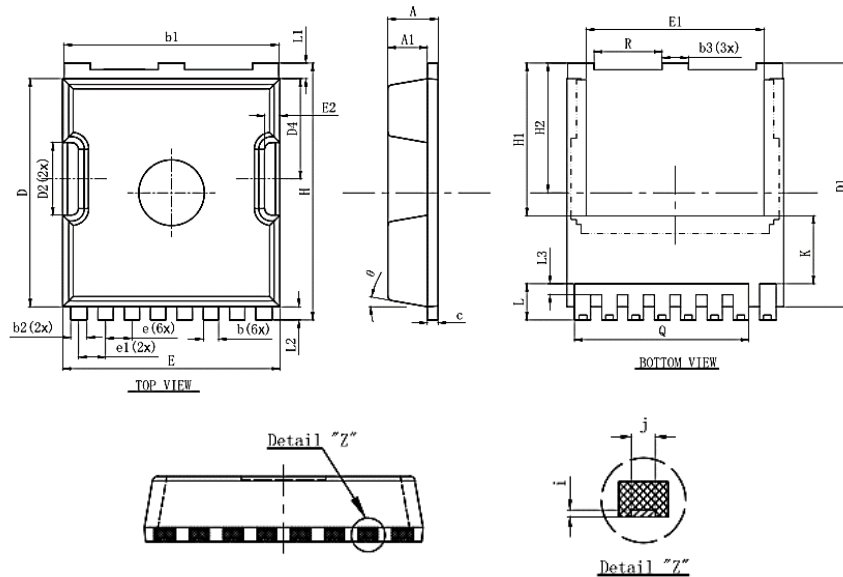


Figure 10: Single Pulse Power Rating, Junction-to-Case



**Package Mechanical Data-TOLLA-8-XZ Single**


Symbol	Dimensions In Millimeters		
	Min.	Nom	Max.
A	2.2	2.3	2.4
A1	1.7	1.8	1.9
b	0.6	0.7	0.8
b1	9.7	9.8	9.9
b2	0.65	0.75	0.85
b3	1.1	1.2	1.3
C	0.4	0.5	0.6
D	10.3	10.4	10.5
D1	11.0	11.1	11.2
D2	3.2	3.3	3.4
D4	4.47	4.57	4.67
E	9.8	9.9	10.0
E1	8.0	8.1	8.2
E2	0.5	0.6	0.7
e	1.200 (BSC)		
e1	1.225 (BSC)		
H	11.6	11.7	11.8
H1	6.95BSC		
H2	5.9BSC		
i	0.1REF		
j	0.350REF		
K	3.100REF		
L	1.55	1.65	1.75
L1	0.6	0.7	0.8
L2	0.5	0.6	0.7
L3	0.4	0.5	0.6
Q	7.95REF		
R	3.0	3.1	3.2
θ	10°REG		

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245°C ±5°C	5sec ±1sec
Pb-Free device	260°C +0/-5°C	5sec ±1sec



This integrated circuit can be damaged by ESD. UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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