



Description

The XPX3400AS-D uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

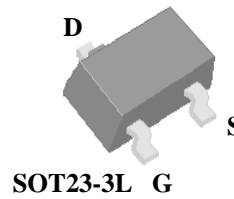
$V_{DS} = 30V, I_D = 7.0A$

$R_{DS(ON)} = 16m\Omega$ (typ) @ $V_{GS} = -10V$

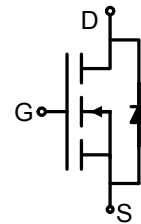
$R_{DS(ON)} = 18m\Omega$ (typ) @ $V_{GS} = 4.5V$

General Features

- High power and current handing capability
- Lead free product is acquired
- Surface mount package
- PWM applications
- Load switch
- Power management



SOT23-3L G



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
XOHV2C	XPX3400AS-D	SOT-23-3L	Ø180mm	8 mm	3000 units

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous	I_D	7.0	A
Drain Current-Pulsed ^(Note 1)	I_{DM}	22	A
Maximum Power Dissipation	P_D	1.4	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$
Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	89	$^\circ C/W$

Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±10V, V _{DS} =0V	-	-	±10	μA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.6	0.9	1.2	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =2.5V, I _D =4A	-	23	35	mΩ
		V _{GS} =4.5V, I _D =5A	-	18	28	mΩ
		V _{GS} =10V, I _D =7.0A	-	16	26	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =5A	10	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, F=1.0MHz	-	597	-	PF
Output Capacitance	C _{oss}		-	66.4	-	PF
Reverse Transfer Capacitance	C _{rss}		-	58.8	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =15V, R _L =2.8Ω V _{GS} =10V, R _{GEN} =3Ω	-	2.8	-	nS
Turn-on Rise Time	t _r		-	2.8	-	nS
Turn-Off Delay Time	t _{d(off)}		-	25	-	nS
Turn-Off Fall Time	t _f		-	4	-	nS
Total Gate Charge	Q _g	V _{DS} =15V, I _D =7.0A , V _{GS} =4.5V	-	9.8	-	nC
Gate-Source Charge	Q _{gs}		-	2.6	-	nC
Gate-Drain Charge	Q _{gd}		-	3.4	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =7.0A	-	-	1.2	V
Diode Forward Current (Note 2)	I _S		-		7.0	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

Typical Electrical and Thermal Characteristics

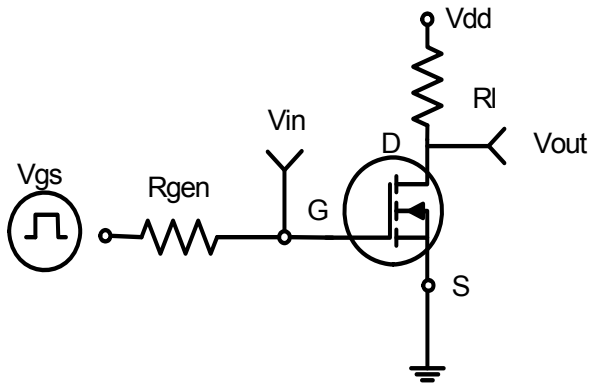


Figure 1: Switching Test Circuit

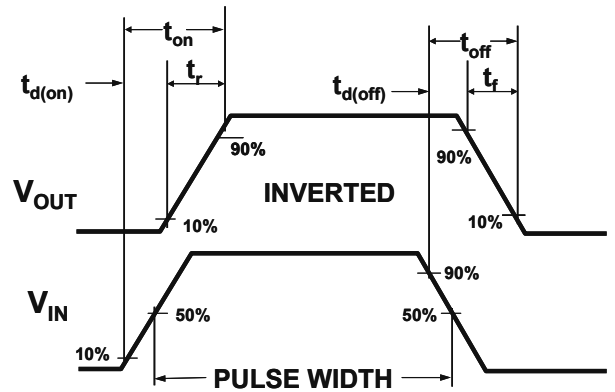


Figure 2: Switching Waveforms

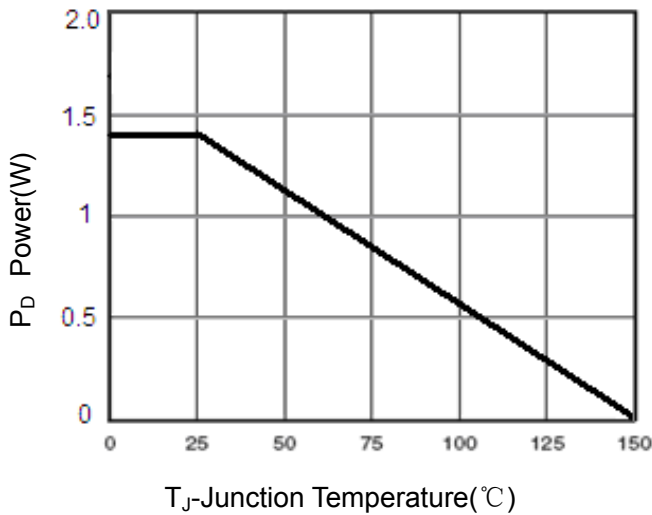


Figure 3 Power Dissipation

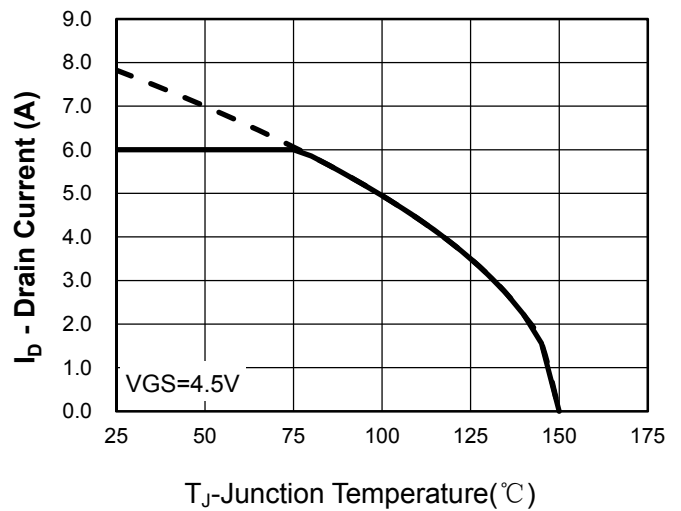


Figure 4 Drain Current

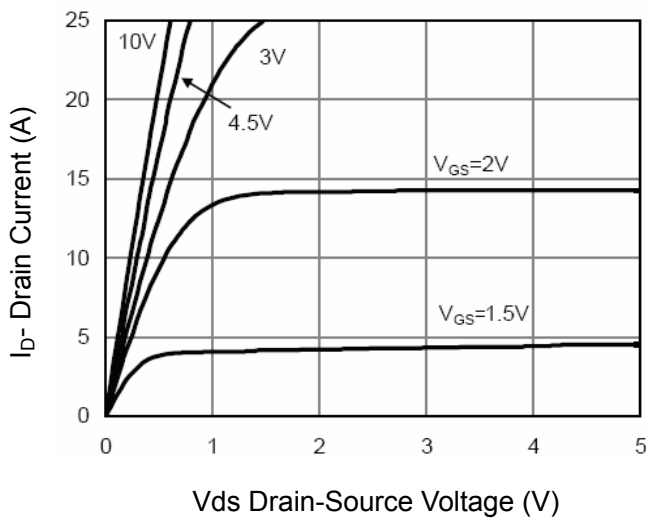


Figure 5 Output Characteristics

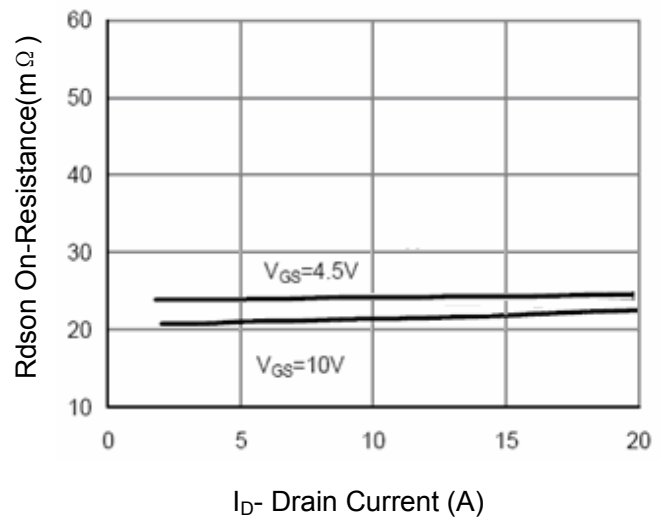


Figure 6 Drain-Source On-Resistance

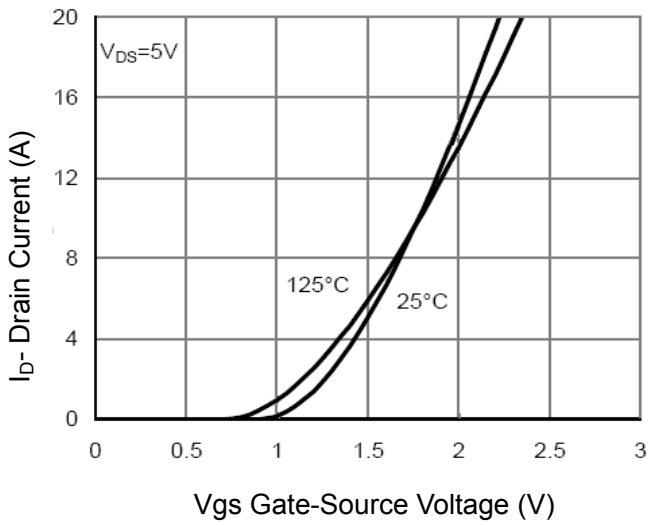


Figure 7 Transfer Characteristics

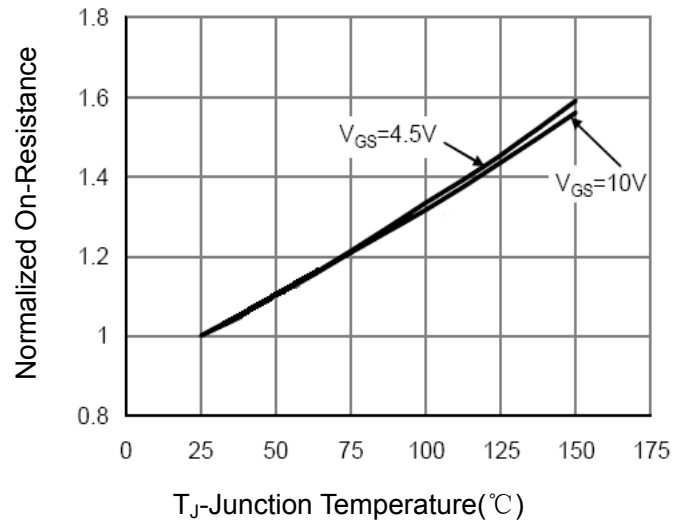


Figure 8 Drain-Source On-Resistance

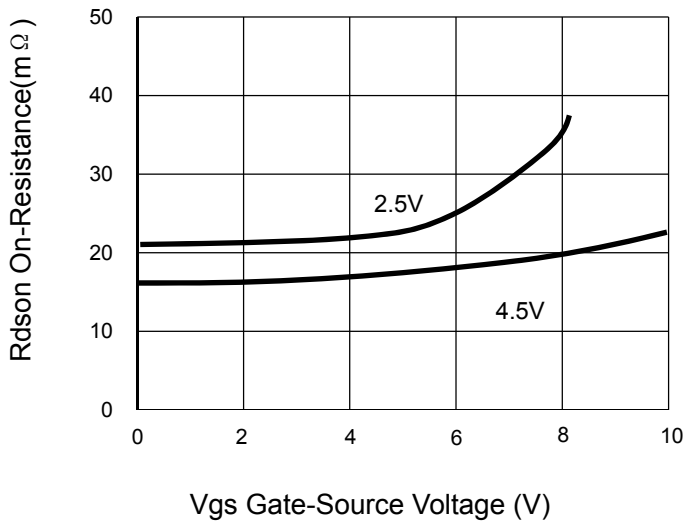


Figure 9 Rdson vs Vgs

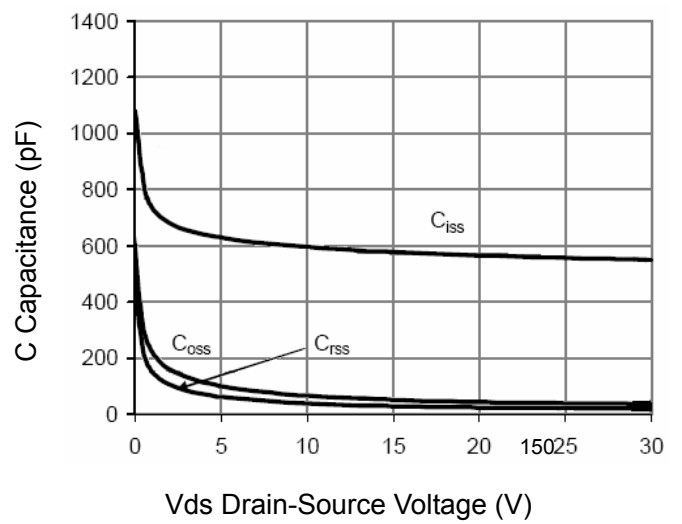


Figure 10 Capacitance vs Vds

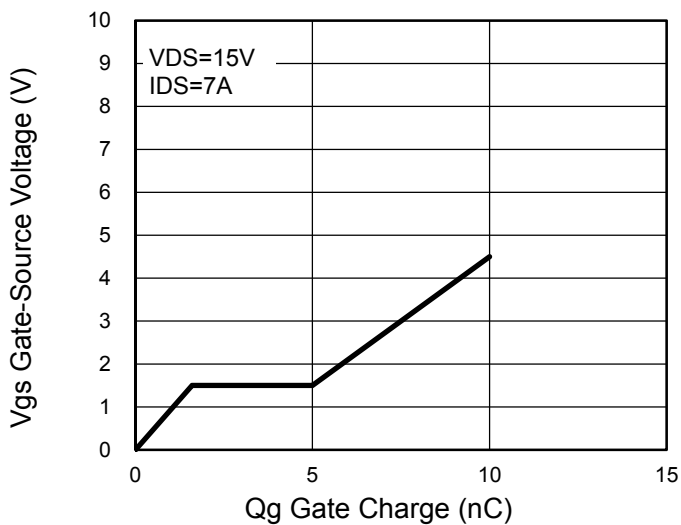


Figure 11 Gate Charge

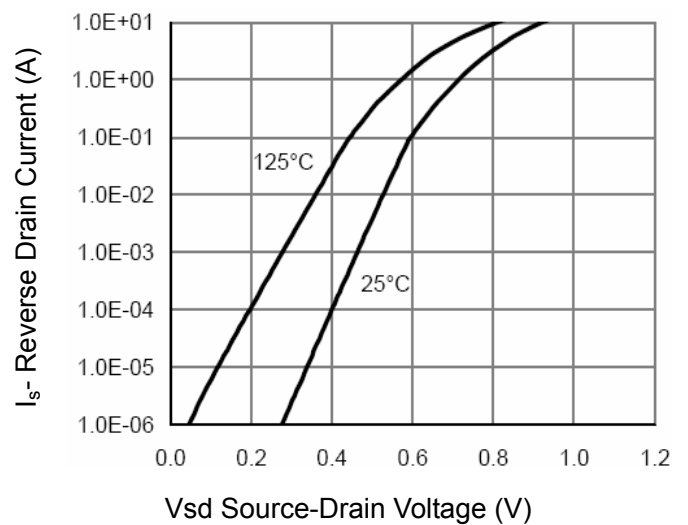


Figure 12 Source-Drain Diode Forward

30V N-Channel Enhancement Mode Power MOSFET

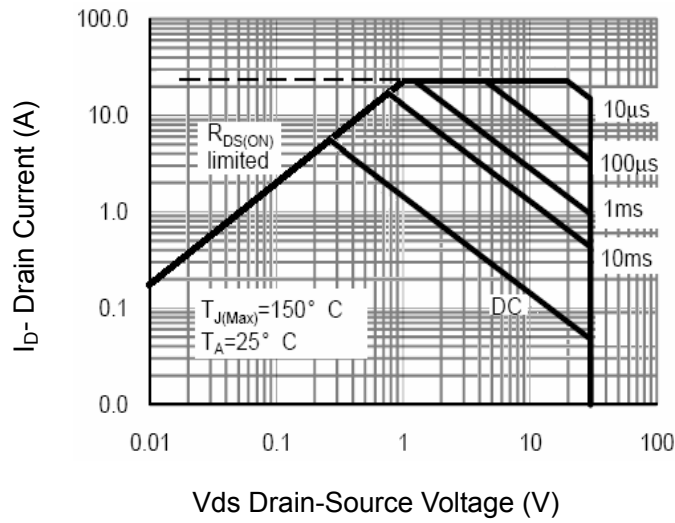


Figure 13 Safe Operation Area

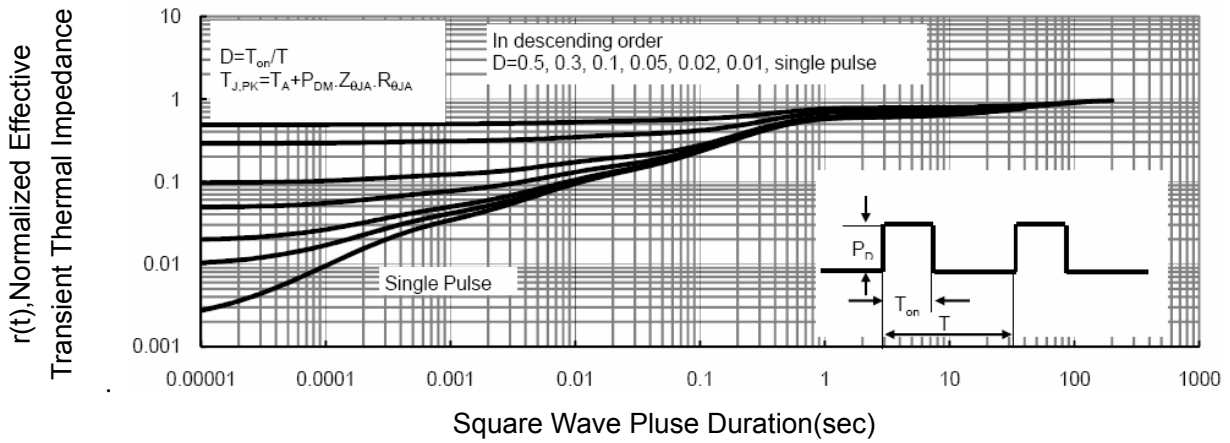
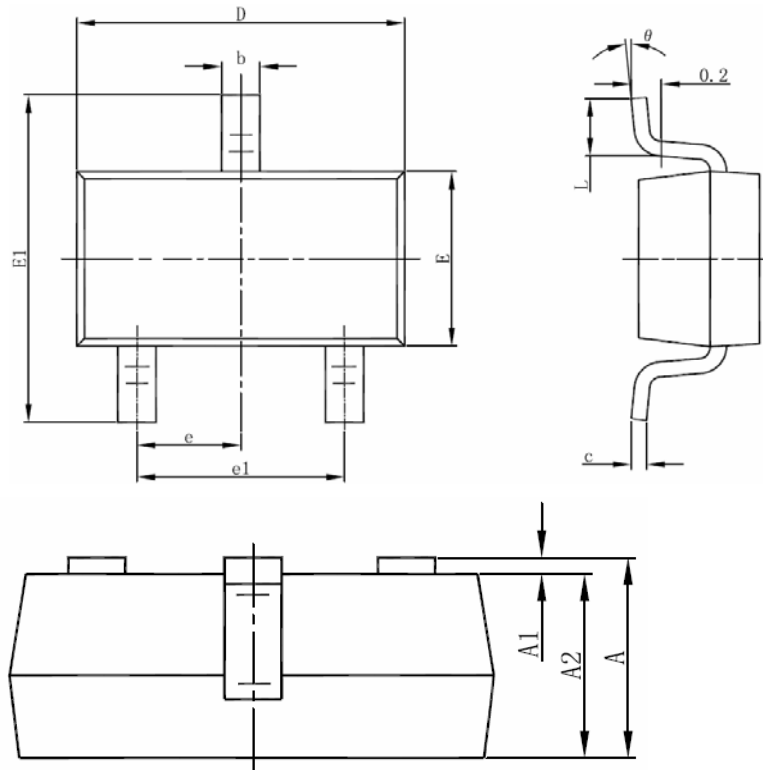


Figure 14 Normalized Maximum Transient Thermal Impedance

SOT-23-3L Package Information


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
theta	0°	8°	0°	8°

Notes

1. All dimensions are in millimeters.
2. Tolerance $\pm 0.10\text{mm}$ (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

30V N-Channel Enhancement Mode Power MOSFET

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245°C ±5°C	5sec±1sec
Pb-Free device	260°C +0/-5°C	5sec±1sec



This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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