



Description

The XPX40200TU uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

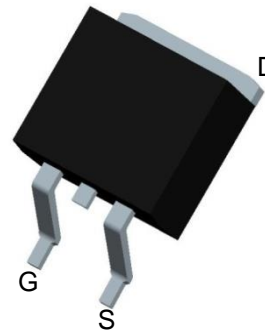
Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

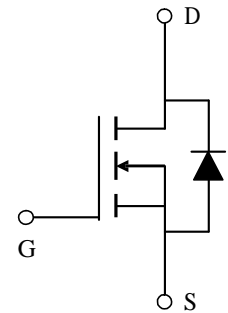
$$V_{DS} = 40V, I_D = 300A$$

$$R_{DS(ON)} = 1.2m\Omega \text{ (typ) @ } V_{GS} = 10V$$

$$R_{DS(ON)} = 1.6m\Omega \text{ (typ) @ } V_{GS} = 4.5V$$



TO-263



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
XPX40200TU	XPX40200TU	TO-263-2L	-	-	-

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	300	A
Drain Current-Continuous ($T_c = 100^\circ C$)	$I_D (100^\circ C)$	235	A
Pulsed Drain Current	I_{DM}	920	A
Maximum Power Dissipation	P_D	370	W
Derating factor		2.5	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	2600	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$
Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.45	$^\circ C/W$

Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	40		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.3	1.8	2.5	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =150A	-	1.2	1.5	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =150A	-	100	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, F=1.0MHz	-	9896	-	PF
Output Capacitance	C _{oss}		-	1460	-	PF
Reverse Transfer Capacitance	C _{rss}		-	1229	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =20V, R _L =15Ω, R _G =2.5Ω, V _{GS} =10V	-	42	-	nS
Turn-on Rise Time	t _r		-	41	-	nS
Turn-Off Delay Time	t _{d(off)}		-	150	-	nS
Turn-Off Fall Time	t _f		-	70	-	nS
Total Gate Charge	Q _g	I _D =150A, V _{DD} =20V, V _{GS} =10V	-	249	-	nC
Gate-Source Charge	Q _{gs}		-	40	-	nC
Gate-Drain Charge	Q _{gd}		-	80	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =150A	-	0.85	1.2	V
Diode Forward Current (Note 2)	I _S		-	-	300	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 300A di/dt = 100A/μs (Note 3)	-	55		nS
Reverse Recovery Charge	Q _{rr}		-	180		nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition: T_J=25°C, V_{DD}=20V, V_G=10V, L=0.5mH, R_G=25Ω

Typical Electrical and Thermal Characteristics (Curves)

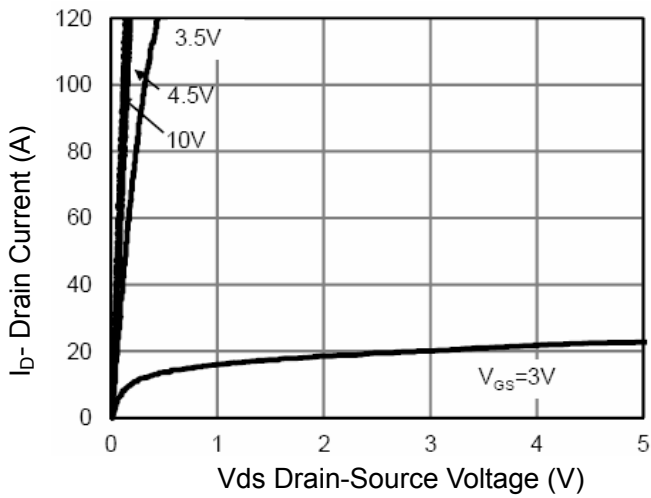


Figure 1 Output Characteristics

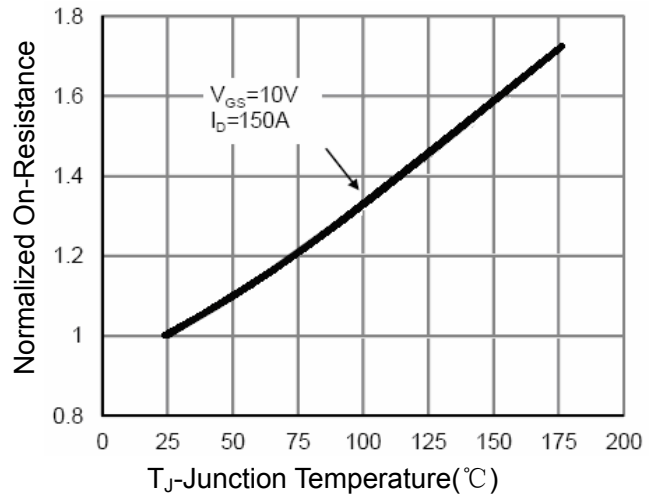


Figure 4 Rds(on)-Junction Temperature

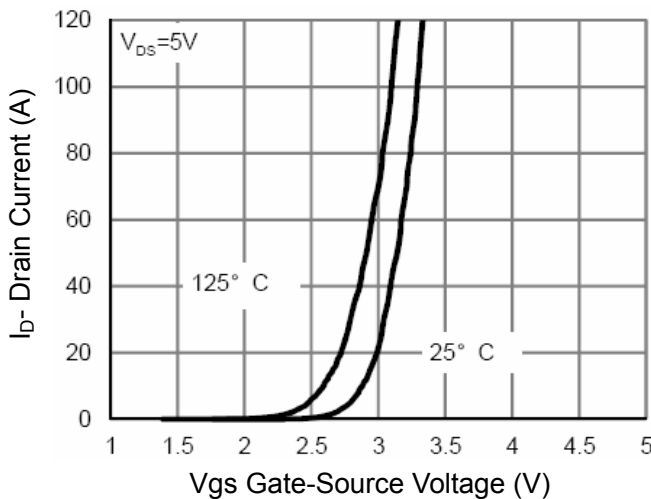


Figure 2 Transfer Characteristics

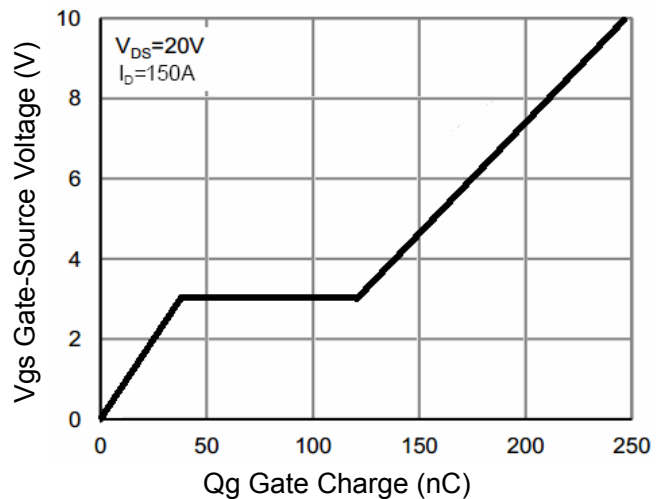


Figure 5 Gate Charge

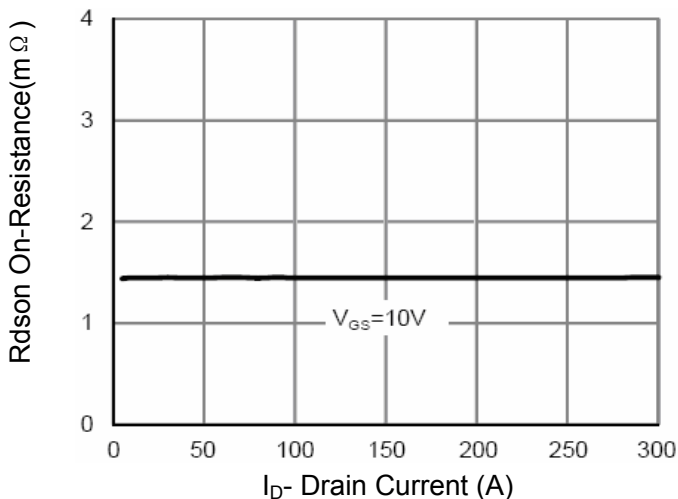


Figure 3 Rds(on)- Drain Current

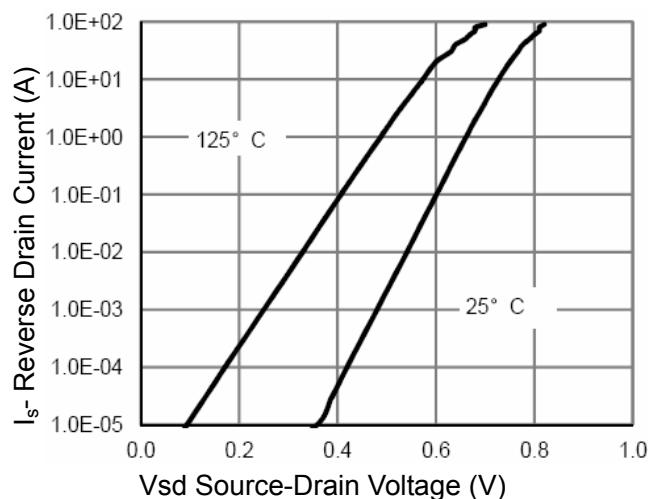


Figure 6 Source- Drain Diode Forward

40V N-Channel Enhancement Mode MOSFET

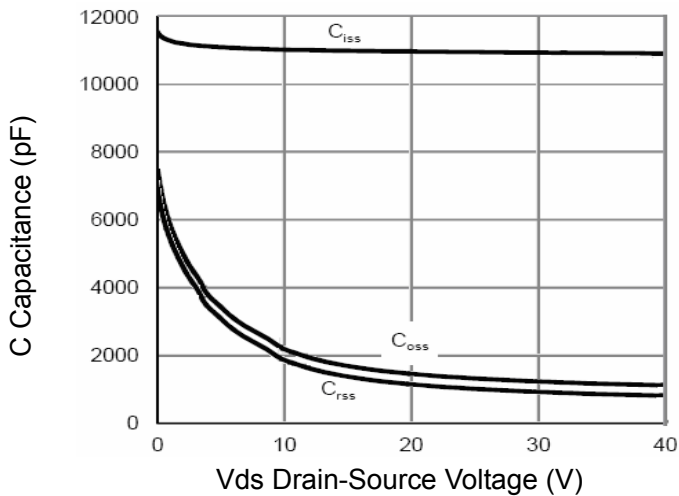


Figure 7 Capacitance vs Vds

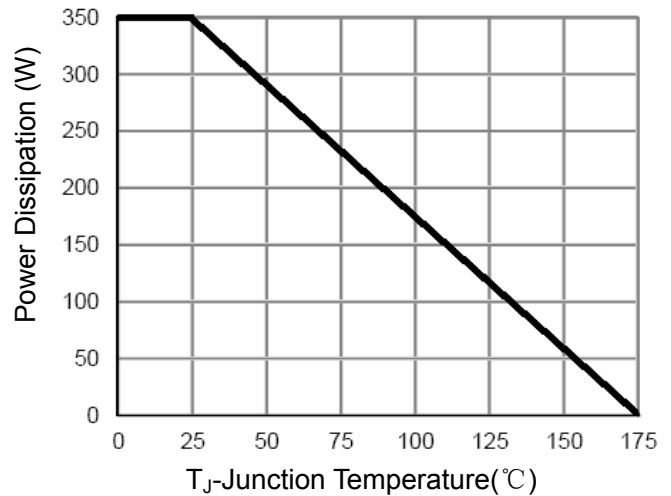


Figure 9 Power De-rating

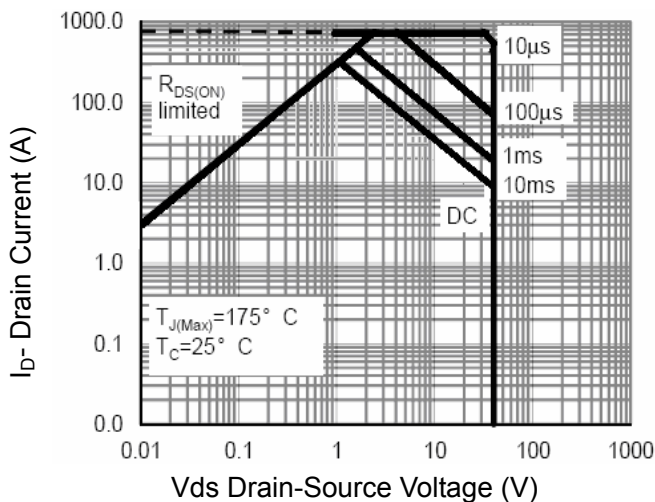


Figure 8 Safe Operation Area

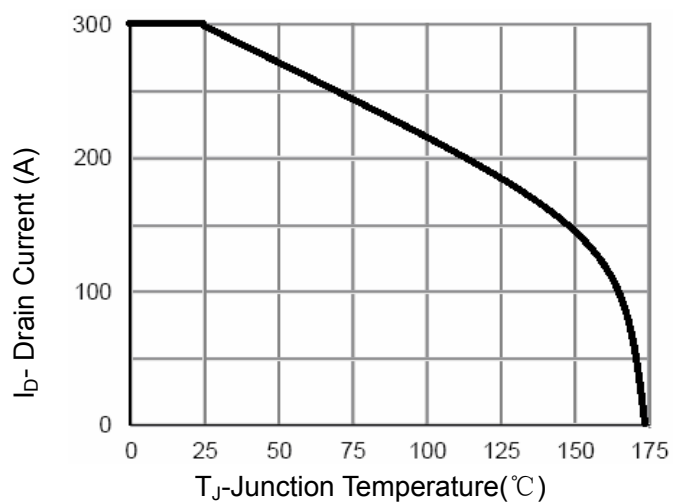


Figure 10 Current De-rating

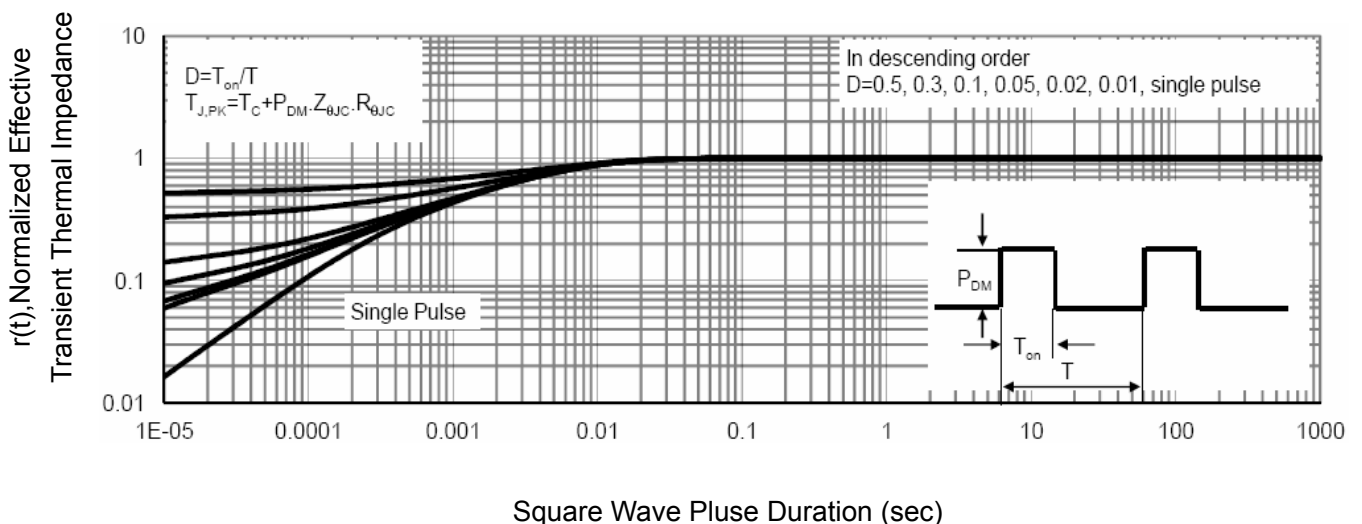
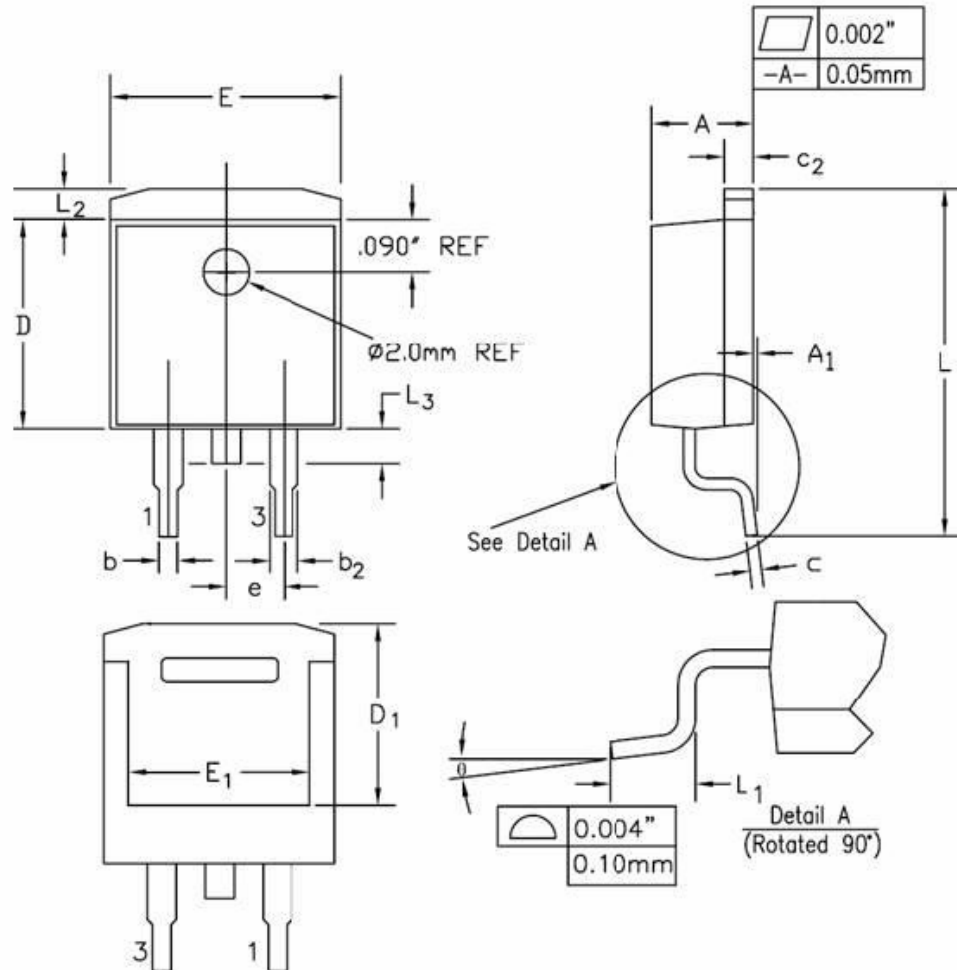


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-263-2L Package Information


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	
A1	-	0.010	-	0.25	
b	0.028	0.037	0.71	0.94	
b2	0.045	0.055	1.15	1.40	
c	0.018	0.024	0.46	0.61	
c2	0.048	0.055	1.22	1.40	
D	0.350	0.370	8.89	9.40	
D1	0.315	0.324	8.01	8.23	
E	0.395	0.405	10.04	10.28	
E1	0.310	0.318	7.88	8.08	
e	0.100 BSC.		2.54 BSC.		
L	0.580	0.620	14.73	15.75	
L1	0.090	0.110	2.29	2.79	
L2	0.045	0.055	1.15	1.39	
L3	0.050	0.070	1.27	1.77	
θ	0°	8°	0°	8°	

40V N-Channel Enhancement Mode MOSFET

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245°C ±5°C	5sec ±1sec
Pb-Free device	260°C +0/-5°C	5sec ±1sec



This integrated circuit can be damaged by ESD. UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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