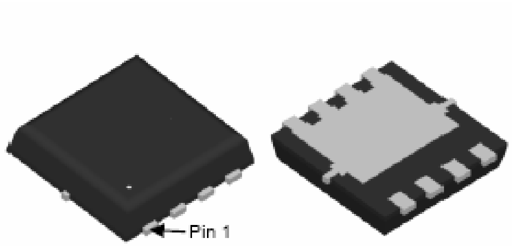
40V N-Channel Enhancement Mode MOSFET

Description

The XPX40N65RX uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g. This device is ideal for high-frequency switching and synchronous rectification.

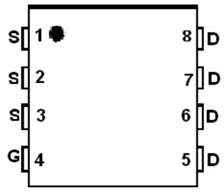


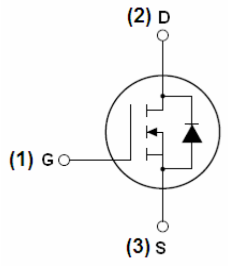
Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

General Features

- V_{DS} =40V,I_D =65A
  $R_{DS(ON)}$=2.3mΩ (typical) @ V_{GS}=10V
  $R_{DS(ON)}$=3.3mΩ (typical) @ V_{GS}=4.5V
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating





Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
4065	4065	DFN3.3X3.3-8L	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous (T_C=25℃)	I_D(T_C=25℃)	65	A
Drain Current-Continuous(T_C=100℃)	I_D (T_C=100℃)	45.5	A
Drain Current-Continuous (T_A=25℃)	I_D(T_A=25℃)	21.5	A
Pulsed Drain Current (Note 1)	I_{DM}	260	A
Maximum Power Dissipation(T_C=25℃)	P_D(T_C=25℃)	55	W
Maximum Power Dissipation(T_A=25℃)	P_D(T_A=25℃)	2.1	W
Derating factor		0.44	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	500	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case(Note 2)	$R_{θJC}$	2.3	℃/W
Thermal Resistance,Junction-to-Ambient(Note 2)	$R_{θJA}$	60	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	40		-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.0	1.5	2.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	2.3	2.8	mΩ
		V_{GS}=4.5V, I_D=20A	-	3.3	4.2	mΩ
Gate resistance	R_G	F=1.0MHz	-	4.0	-	Ω
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=20A		60	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=20V,V_{GS}=0V, F=1.0MHz	-	2110	-	PF
Output Capacitance	C_{oss}		-	777	-	PF
Reverse Transfer Capacitance	C_{rss}		-	15.5	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=20V,I_D=20A V_{GS}=10V,R_G=1.6Ω	-	7.5	-	nS
Turn-on Rise Time	t_r		-	4.0	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	37	-	nS
Turn-Off Fall Time	t_f		-	7.5	-	nS
Total Gate Charge	Q_g	V_{DS}=20V,I_D=20A, V_{GS}=10V	-	34.8	-	nC
Gate-Source Charge	Q_{gs}		-	6.2		nC
Gate-Drain Charge	Q_{gd}		-	5.1		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=20A	-		1.2	V
Diode Forward Current (Note 2)	I_S		-	-	65	A
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = I_S di/dt = 100A/μs(Note3)	-	14	-	nS
Reverse Recovery Charge	Qrr		-	21	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. The value of $R_{θJA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition : Tj=25℃,V_{DD}=20V,V_G=10V,L=0.5mH,Rg=25Ω

Typical Electrical and Thermal Characteristics

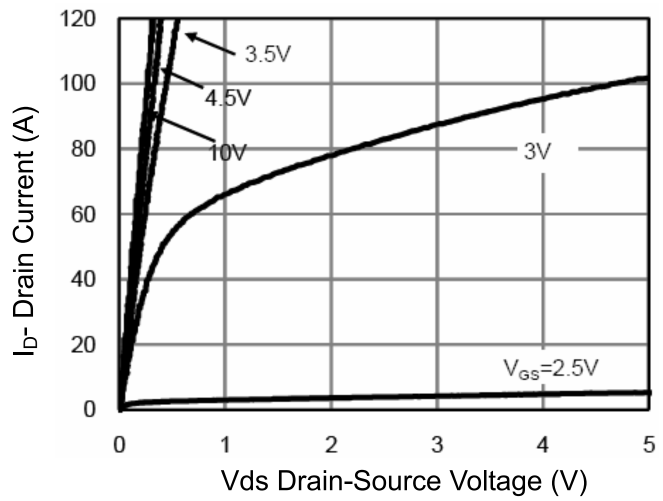


Figure 1 Output Characteristics

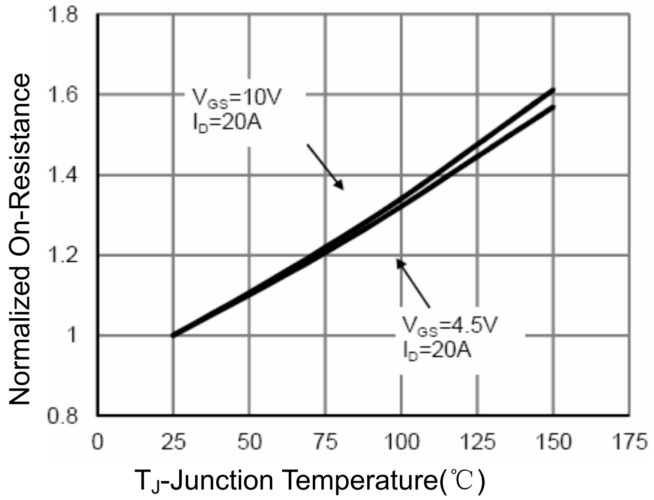


Figure 4 Rdson-Junction Temperature

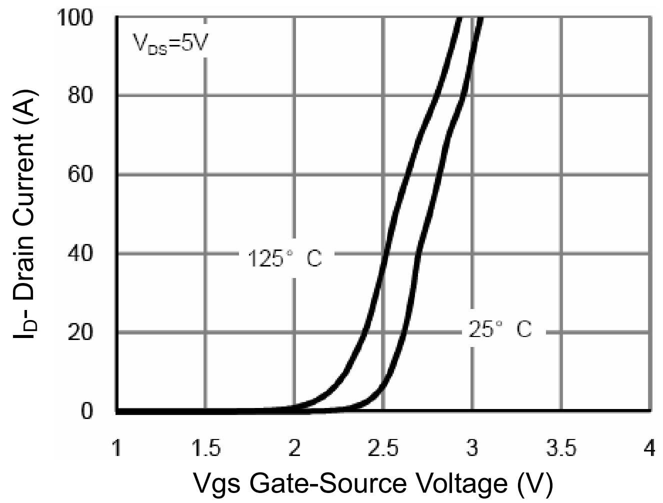


Figure 2 Transfer Characteristics

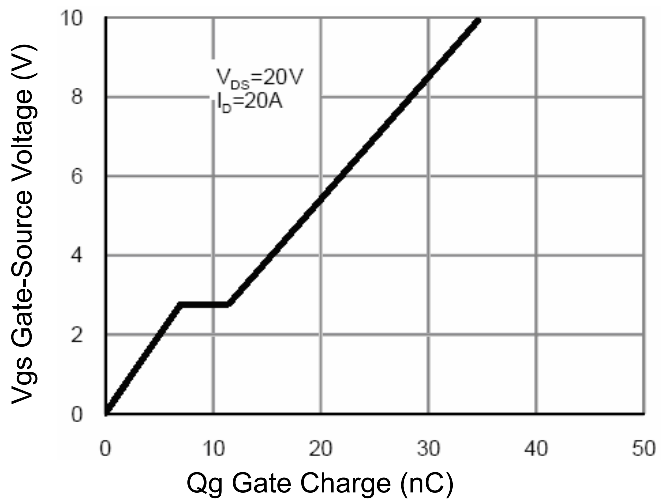


Figure 5 Gate Charge

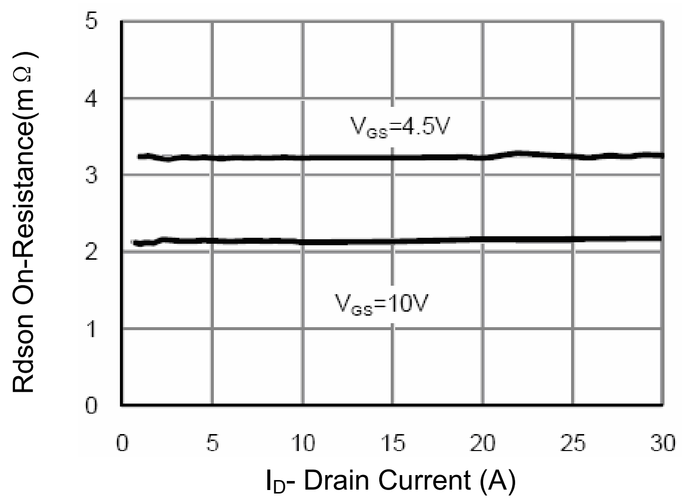


Figure 3 Rdson- Drain Current

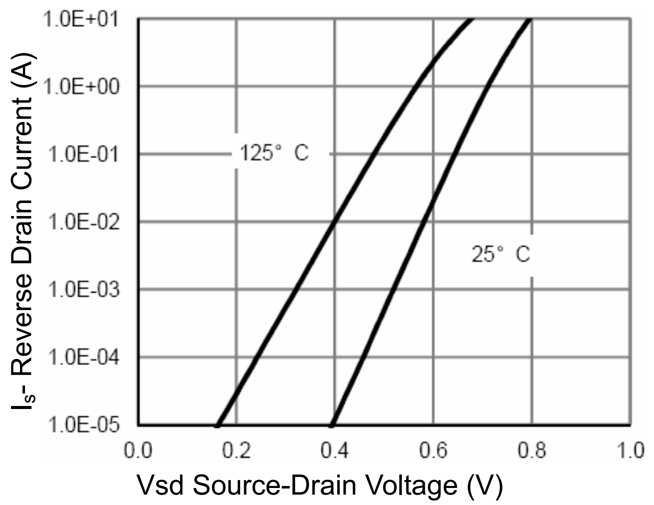


Figure 6 Source- Drain Diode Forward

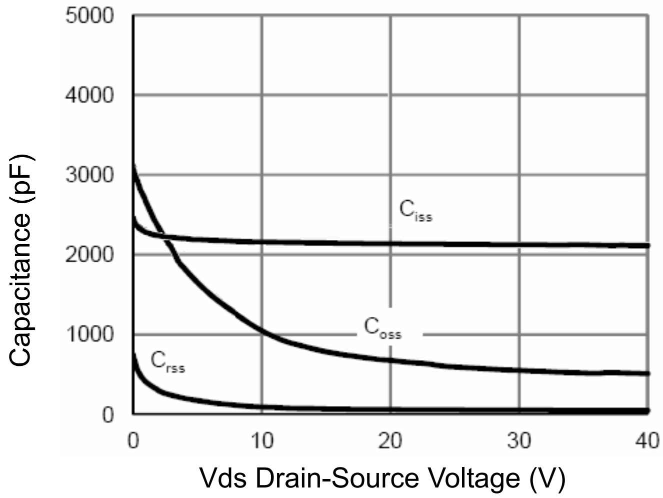


Figure 7 Capacitance vs Vds

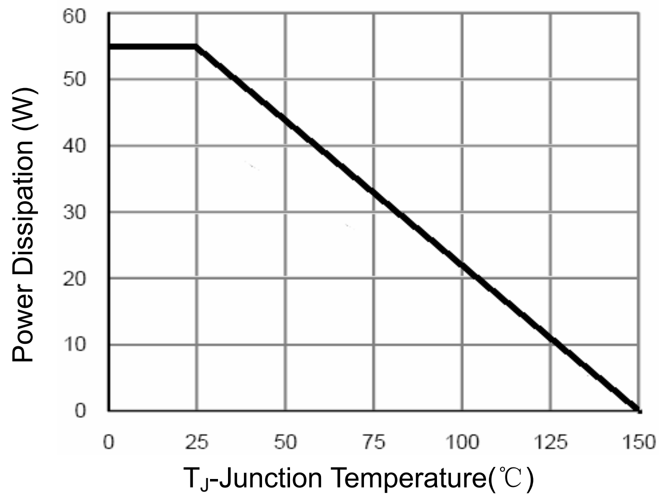


Figure 9 Power De-rating

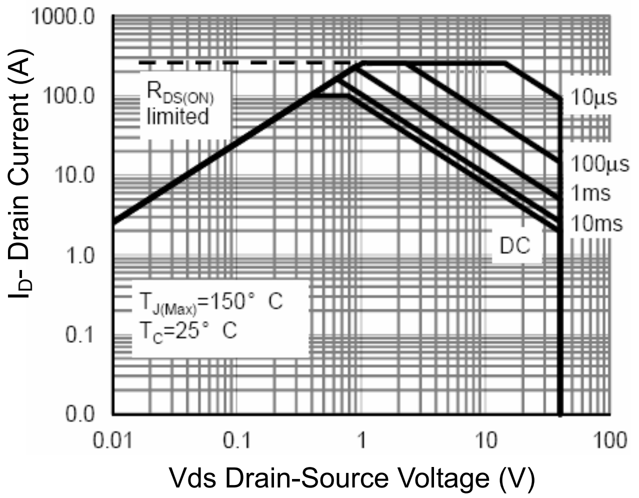


Figure 8 Safe Operation Area

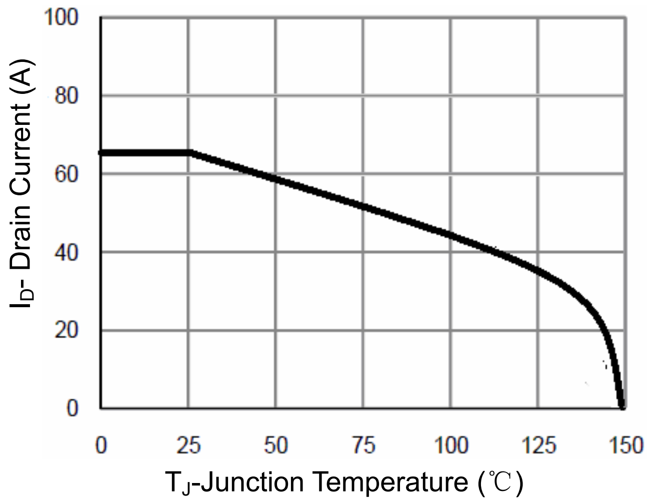


Figure 10 Current De-rating

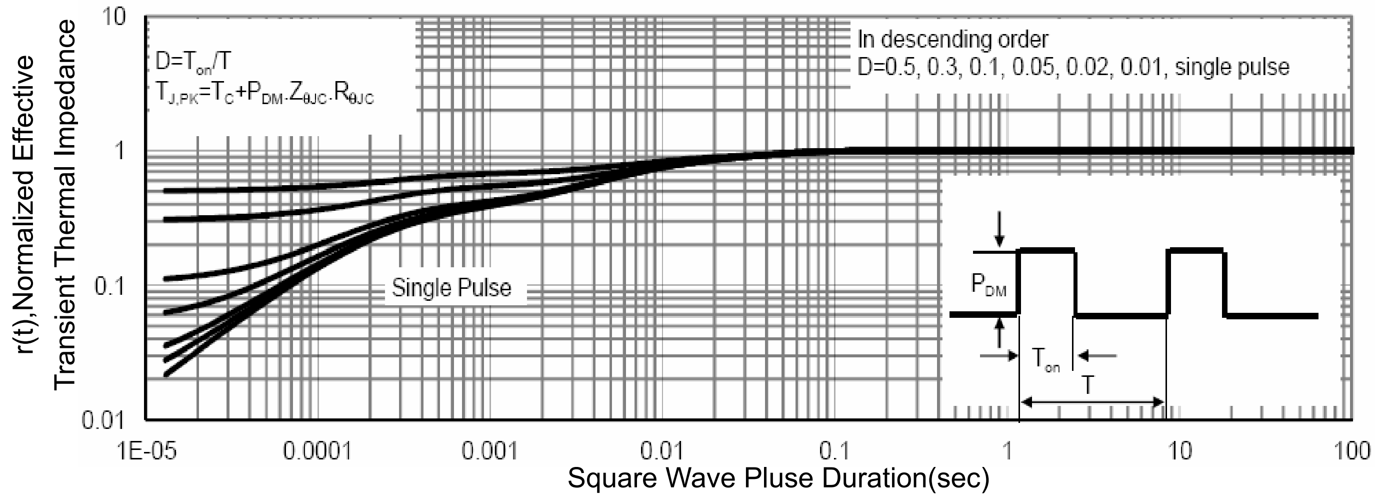
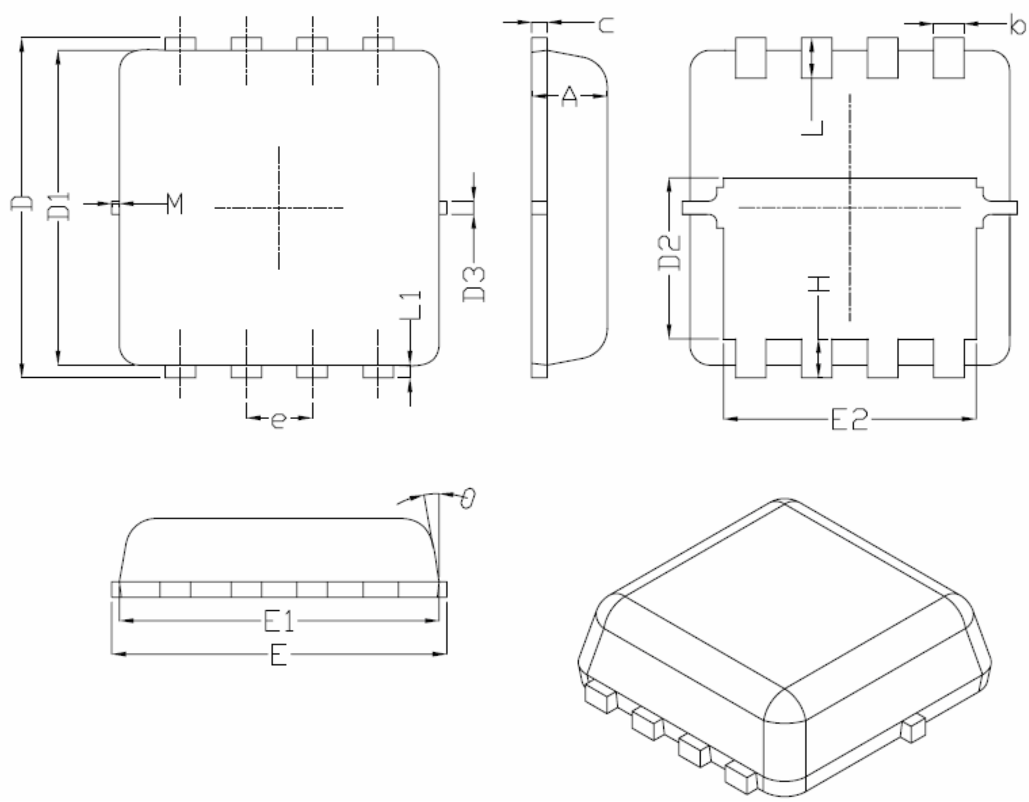


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN3.3X3.3-8L Package Information



Symbol	Dimensions In Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.48	1.58	1.68
D3	-	0.13	-
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	-	0.13	-
M	*	*	0.15
θ		10°	12°

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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