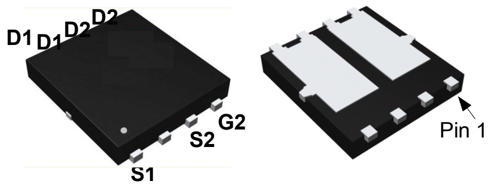
40V N+P-Channel Enhancement Mode MOSFET

Description

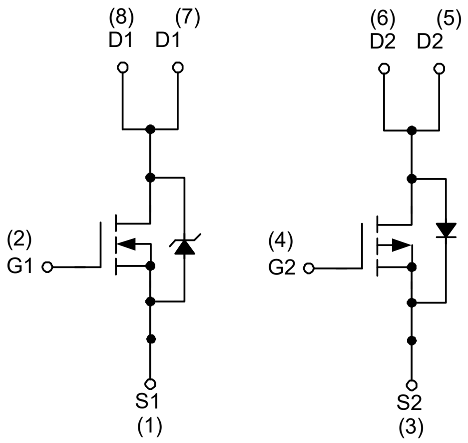
The XPX45NP04RD uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection

or in other Switching application.

Pin Description



DFN5x6C-8_EP2



N-Channel MOSFET P-Channel MOSFET

General Features

V_{DS} = 40V I_D =45A

$R_{DS(ON)}$ < 7mΩ @ V_{GS}=10V

V_{DS} = -40V I_D =-40A

$R_{DS(ON)}$ < 10mΩ @ V_{GS}=-10V

Application

Wireless charging

Boost driver

Brushless motor

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
XPX45NP04RD	PDFN5*6-8L	XPX45NP04RD XXX YYYY	5000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	N-Ch	P-Ch	Units
V_{DS}	Drain-Source Voltage	40	-40	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	45	-40	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V[1]	32.5	-27.5	A
I_{DM}	Pulsed Drain Current[2]	123	-115	A
EAS	Single Pulse Avalanche Energy[3]	289	378	mJ
I_{AS}	Avalanche Current	42	50	A
P_D@T_C=25℃	Total Power Dissipation[4]	46	41.3	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	℃
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	25		℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	2.3		℃/W

N-Electrical Characteristics (T_C=25℃unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	40	44	---	V
△BVDSS/△TJ	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	0.034	---	V/℃
RDS(ON)	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=10A	---	7.0	10	mΩ
		V_{GS}=4.5V , I_D=8A	---	9.0	12	
VGS(th)	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	1.0	1.6	2.5	V
△$V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.96	---	mV/℃
IDSS	Drain-Source Leakage Current	V_{DS}=32V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=32V , V_{GS}=0V , T_J=55℃	---	---	5	
IGSS	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=5V , I_D=10A	---	40	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	1.6	---	Ω
Q_g	Total Gate Charge (4.5V)	V_{DS}=20V , V_{GS}=4.5V , I_D=10A	---	18.8		nC
Qgs	Gate-Source Charge		---	4.7		
Qgd	Gate-Drain Charge		---	8.2		
Td(on)	Turn-On Delay Time	V_{DD}=15V , V_{GS}=10V , R_G=3.3Ω I_D=1A	---	14.3		ns
T_r	Rise Time		---	2.6		
Td(off)	Turn-Off Delay Time		---	77		
T_f	Fall Time		---	4.8		
Ciss	Input Capacitance	V_{DS}=15V , V_{GS}=0V , f=1MHz	---	2333		pF
Coss	Output Capacitance		---	193		
Crss	Reverse Transfer Capacitance		---	138		
IS	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	10.5	A
ISM	Pulsed Source Current[2,5]		---	---	42	A
VSD	Diode Forward Voltage[2]	V_{GS}=0V , I_S=1A , T_J=25℃	---	---	1	V

Note :

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width .The EAS data shows Max. rating .

3、The power dissipation is limited by 175℃ junction temperature

4、EAS condition: TJ=25℃, VDD=32V, VG= 10V, RG=25Ω, L=0.1mH, IAS= 25A

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

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P-Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-40	-44	---	V
$\triangle BV_{DSS}/\triangle T_J$	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.023	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V , I_D=-30A	---	10	13	mΩ
		V_{GS}=-4.5V , I_D=-20A	---	15	20	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D=-250uA	-1.0	-1.6	-2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.74	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-40V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=-40V , V_{GS}=0V , T_J=55℃	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-20V , V_{GS}=-4.5V , I_D=-12A	---	25	---	nC
Q_{gs}	Gate-Source Charge		---	11	---	
Q_{gd}	Gate-Drain Charge		---	9.5	---	
$T_{d(on)}$	Turn-On Delay Time	VDD =-15V, RL=15Ω ID =-1A, VGEN =-10V, RG =6Ω	---	48	---	ns
T_r	Rise Time		---	24	---	
$T_{d(off)}$	Turn-Off Delay Time		---	88	---	
T_f	Fall Time		---	9.6	---	
C_{iss}	Input Capacitance	V_{DS}=-20V , V_{GS}=0V , f=1MHz	---	2760	---	pF
C_{oss}	Output Capacitance		---	260	---	
C_{rss}	Reverse Transfer Capacitance		---	85	---	
I_S	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	-40	A
I_{SM}	Pulsed Source Current[2,5]		---	---	-90	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1.3	V

Note :

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width .The EAS data shows Max. rating .

3、The power dissipation is limited by 175℃ junction temperature

4、EAS condition: TJ=25℃, VDD= -24V, VG= -10V, RG=7Ω, L=0.1mH, IAS= -29A

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

N-Typical Characteristics

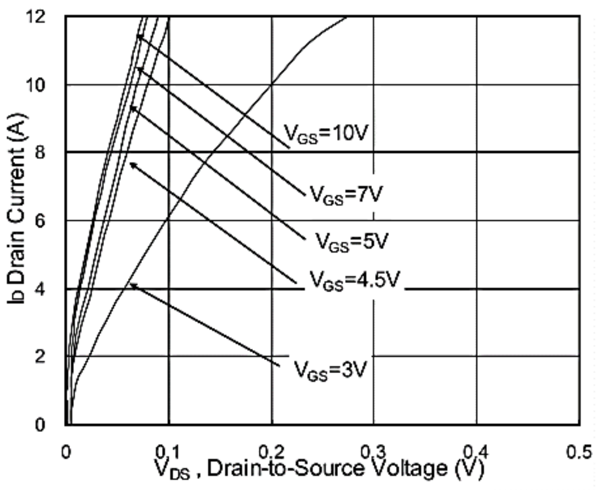


Fig.1 Typical Output Characteristics

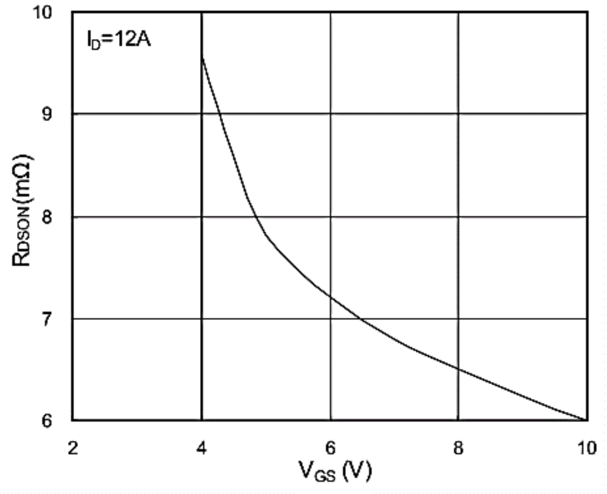


Fig.2 On-Resistance vs. G-S Voltage

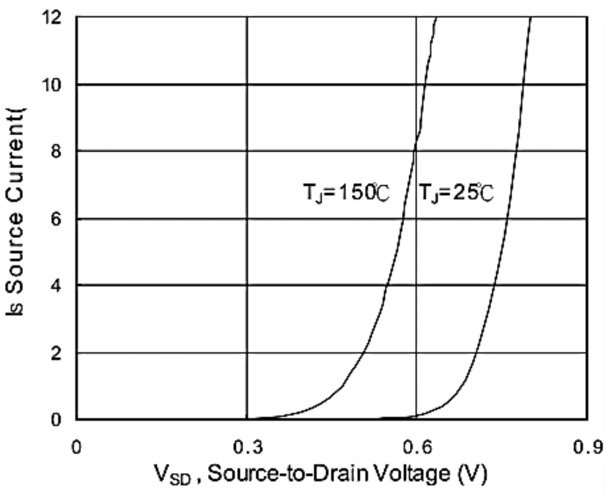


Fig.3 Forward Characteristics of Reverse

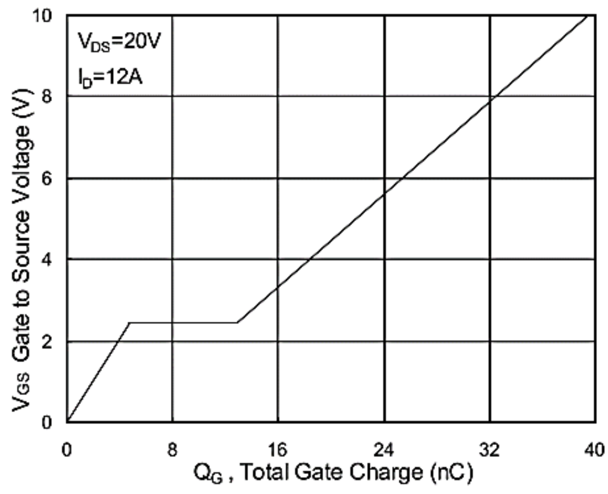


Fig.4 Gate-Charge Characteristics

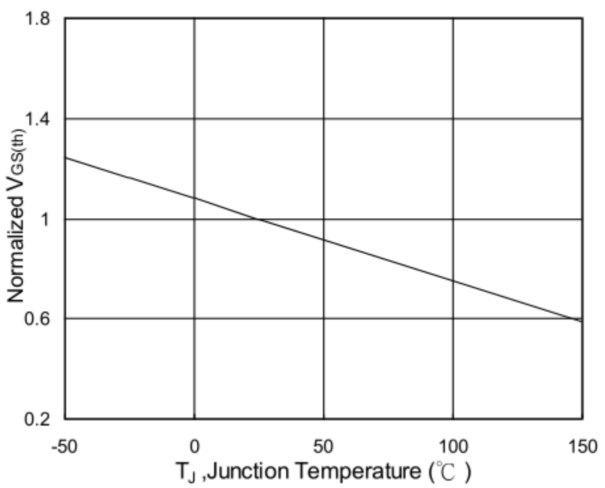


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

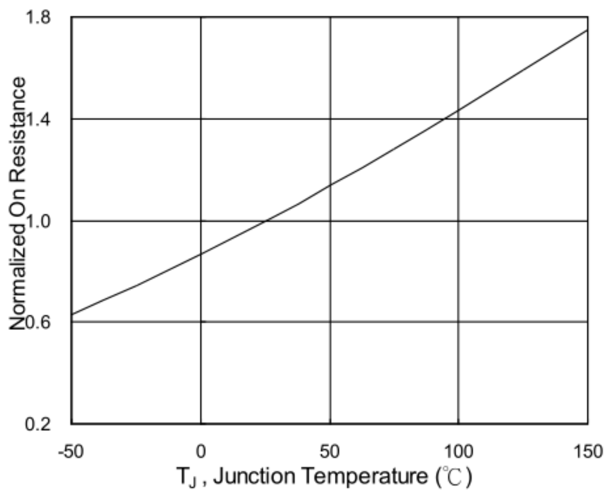


Fig.6 Normalized R_{DSON} vs. T_J

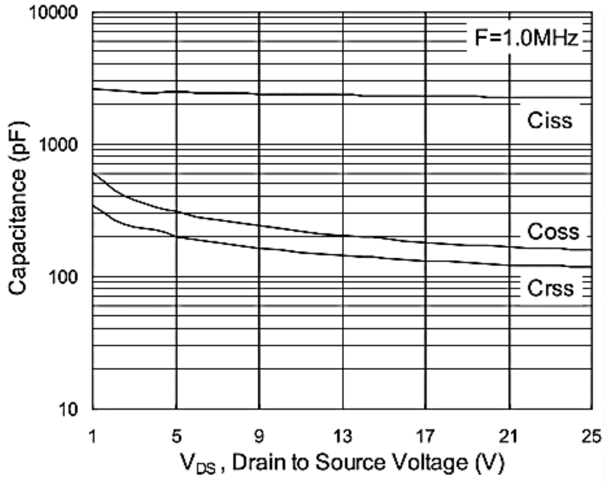


Fig.7 Capacitance

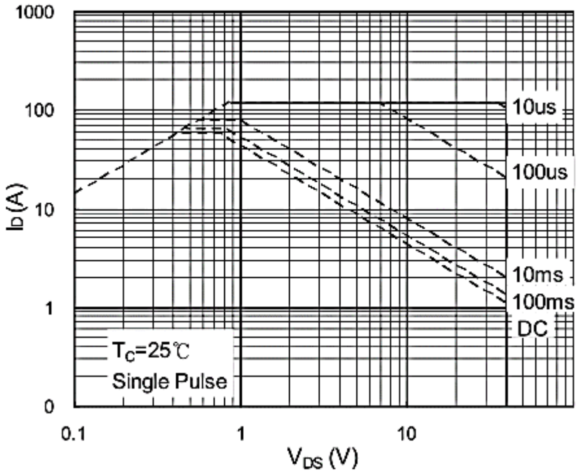


Fig.8 Safe Operating Area

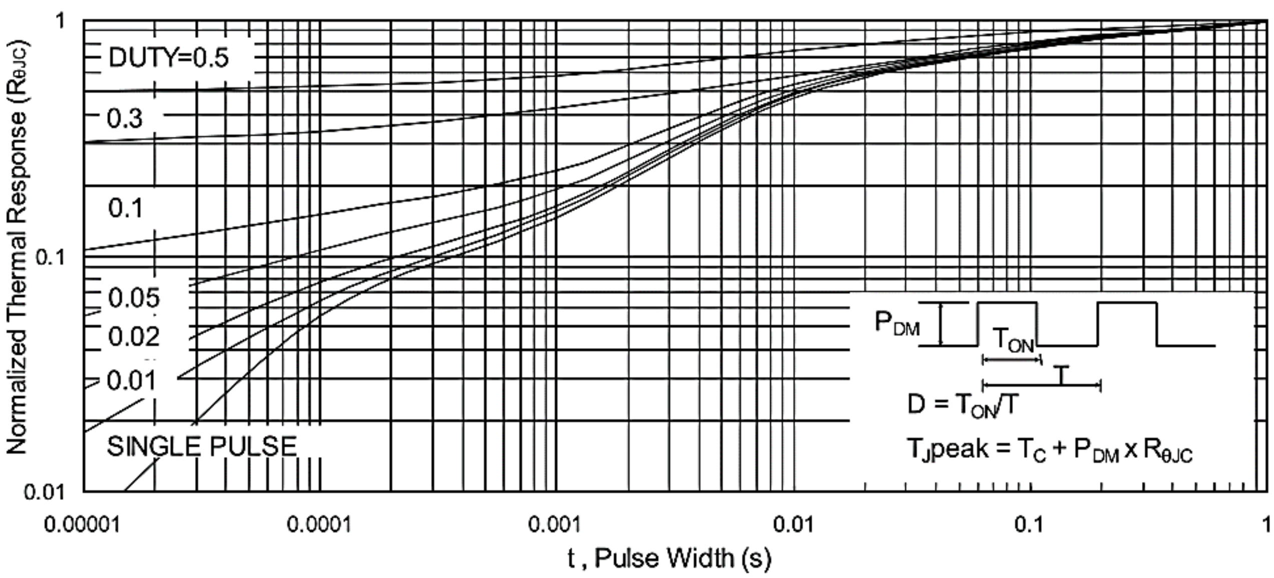


Fig.9 Normalized Maximum Transient Thermal Impedance

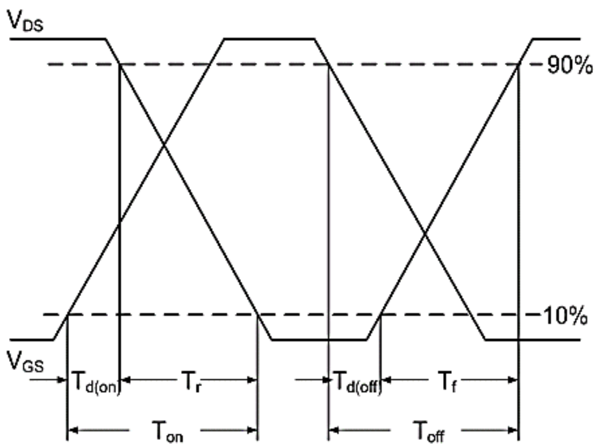


Fig.10 Switching Time Waveform

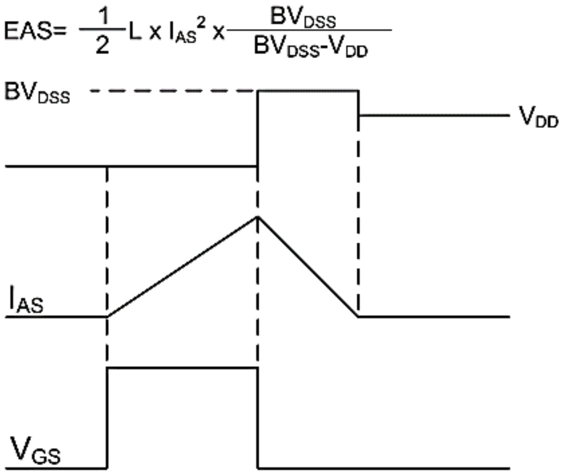


Fig.11 Unclamped Inductive Waveform

P-Typical Characteristics

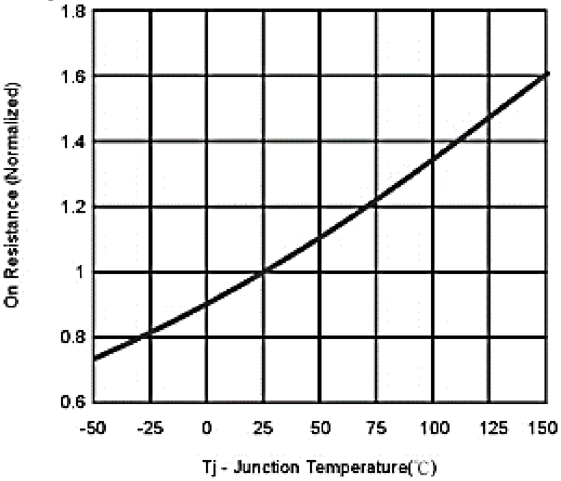


Fig.1 On Resistance Vs Junction Temperature

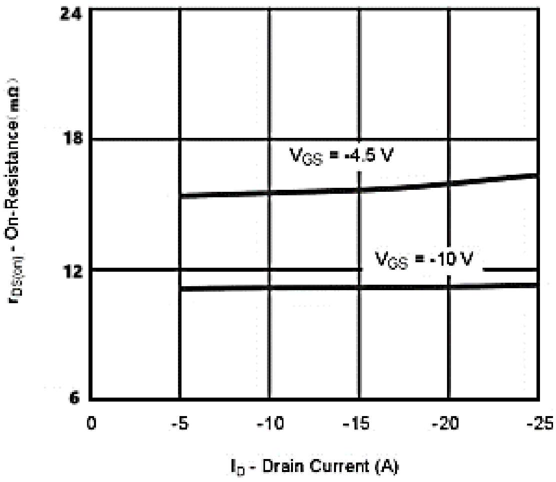


Fig.2 On-Resistance Vs.Drain Current

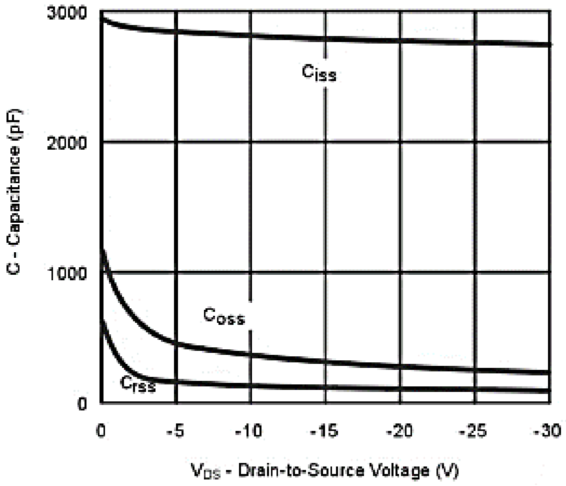


Fig.3 Capacitance

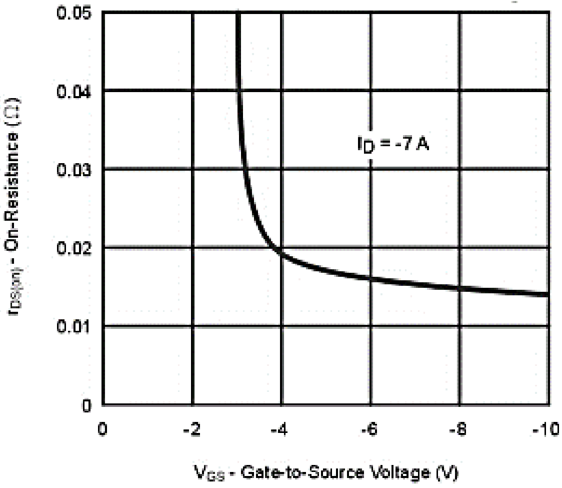


Fig.4 On-Resistance Vs. Gate-to-Sourece Voltage

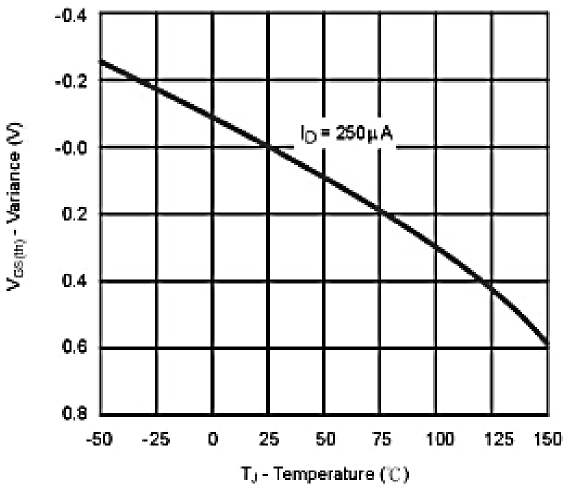


Fig.5 Threshold Voltage

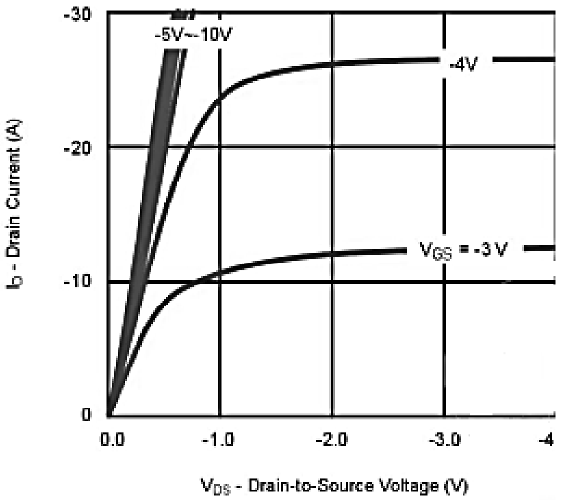


Fig.6 On-Region Characteristics

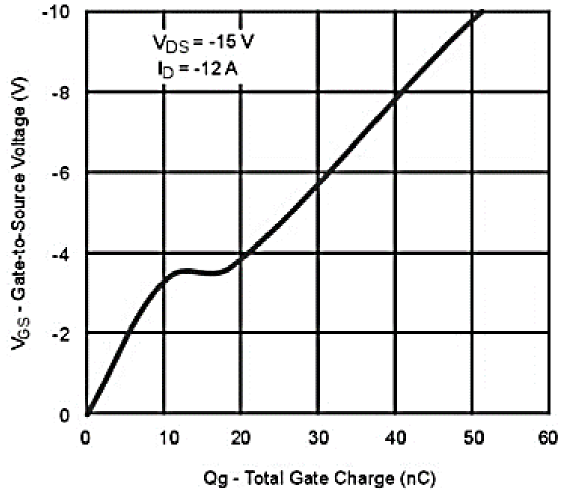


Fig.7 Gate Charge

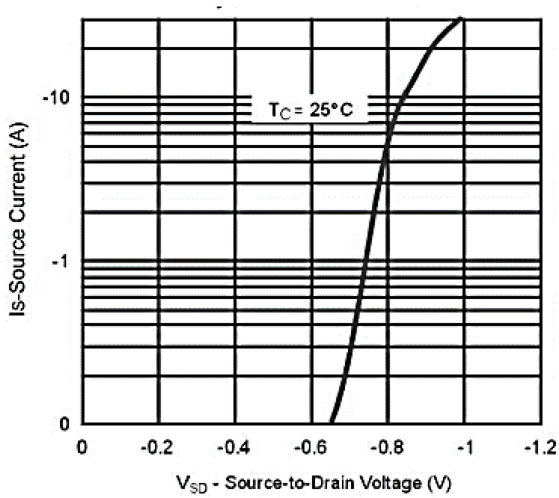


Fig.8 Body-diode Characteristice

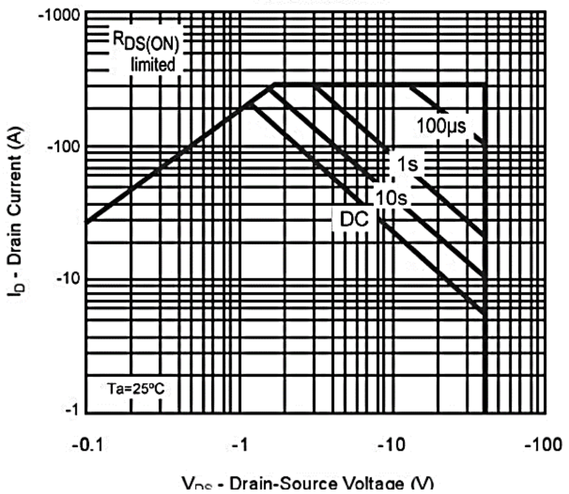


Fig.9 Safe Operating Area

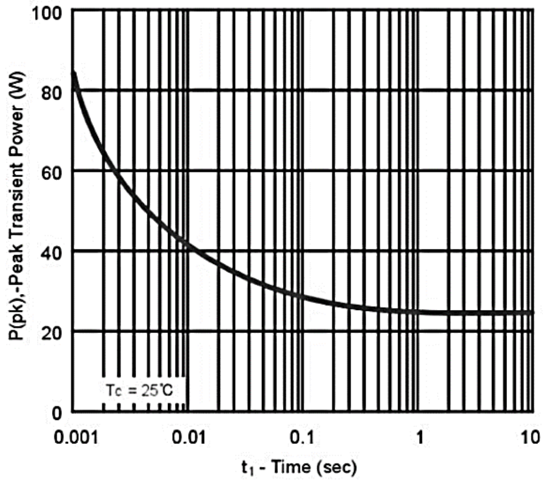


Fig.10 Single Pluse Maximum Power Dissipation

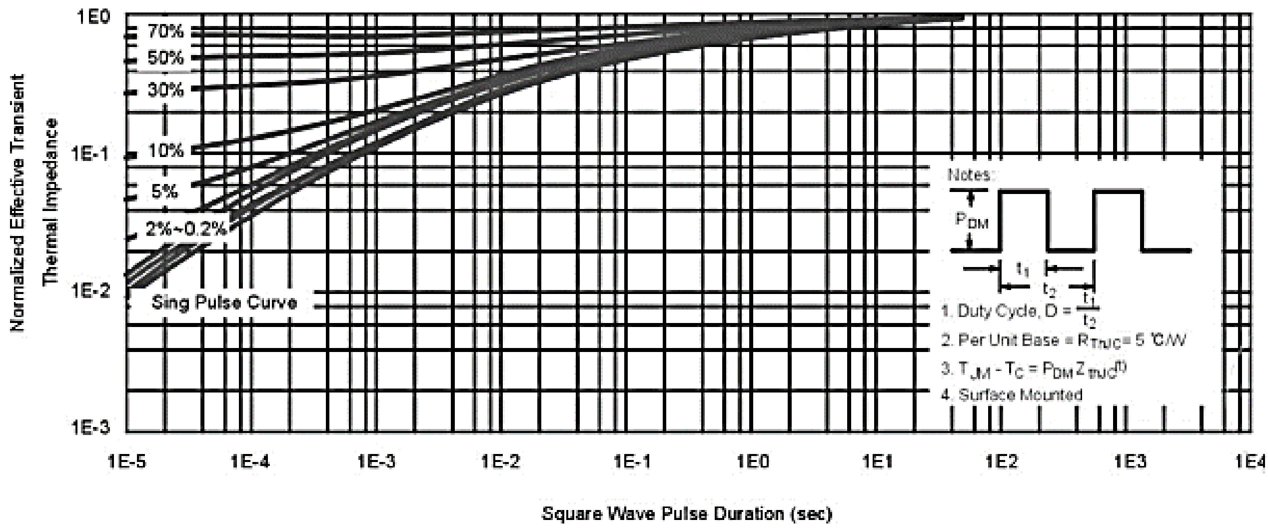
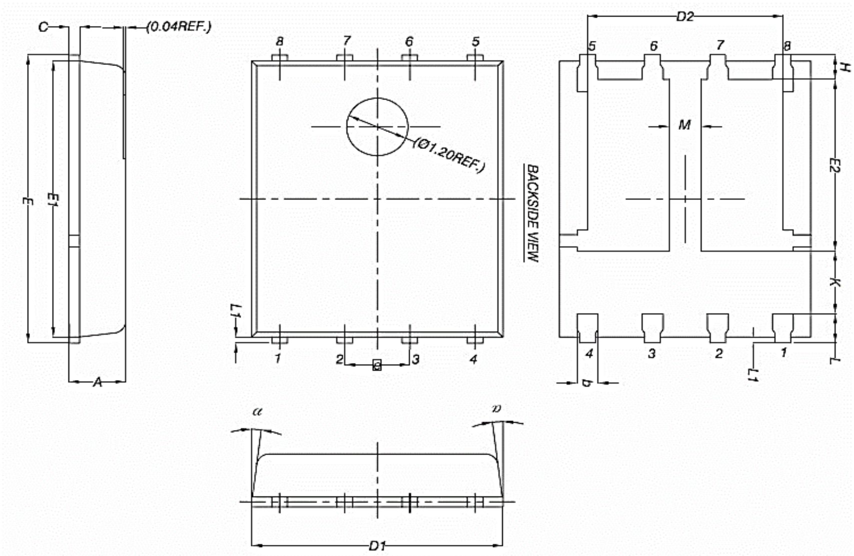


Fig.11 Normalized Maximum Transient Thermal Impedance

Package Mechanical Data-DFN5*6-8L-JQ Double



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	3.30	3.45
E2	3.38	3.05	3.20
e	1.27BSC		
H	0.41	0.51	0.61
K	1.10	--	--
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
M	0.50	--	--
a	0°	--	12°

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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