XPX60P100

-55V P-Channe Enhancement Mode Power MOSFET

RoHS COMPLIANT

Description

The XPX60P100 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

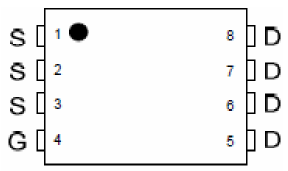
V_{DS} =-55V,I_D =-100A
$R_{DS(ON)}$=10mΩ@V_{GS}=-10V
$R_{DS(ON)}$=13mΩ@V_{GS}=-4.5V

General Features

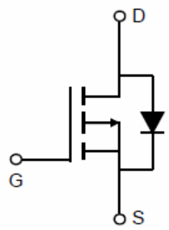
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

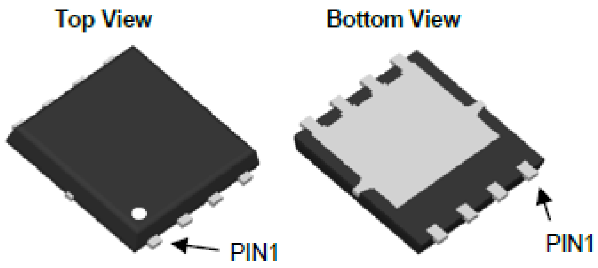
- Load switch
- Battery protection



Pin Assignment



Schematic diagram



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
XPX60P100	XPX60P100	DFN5X6-8L	-	-	5000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-55	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	-100	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	-58	A
Pulsed Drain Current	I_{DM}	-200	A
Maximum Power Dissipation	P_D	82	W
Derating factor		0.63	W/℃
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃
Thermal Resistance,Junction-to-Case(Note 2)	$R_{θJC}$	1.6	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-55	-60	---	V
△BVDSS/△TJ	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.035	---	V/℃
RDS(ON)	Static Drain-Source On-Resistance[2]	V_{GS}=-10V , I_D=-20A	---	10	12	mΩ
		V_{GS}=-4.5V , I_D=-15A	---	13	16	
VGS(th)	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-1.2	-1.8	-2.5	V
△$V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.3	---	mV/℃
IDSS	Drain-Source Leakage Current	V_{DS}=-60V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=-60V , V_{GS}=0V , T_J=55℃	---	---	5	
IGSS	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-20A	---	48	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	2.2	---	Ω
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-30V , V_{GS}=-10V , I_D=-20A	---	59	---	nC
Q_{gs}	Gate-Source Charge		---	13	---	
Q_{gd}	Gate-Drain Charge		---	10	---	
Td(on)	Turn-On Delay Time	V_{DD}=-30V , V_{GS}=-10V , R_G=3Ω, I_D=-20A	---	4.5	---	ns
T_r	Rise Time		---	2.5	---	
Td(off)	Turn-Off Delay Time		---	14.5	---	
T_f	Fall Time		---	3.8	---	
C_{iss}	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	3980	---	pF
Coss	Output Capacitance		---	600	---	
Crss	Reverse Transfer Capacitance		---	25	---	
I_S	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	-100	A
ISM	Pulsed Source Current[2,5]		---	---	-260	A
VSD	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1.2	V

Note :

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The EAS data shows Max. rating . The test condition is VDD =-48V,VGS =-10V,L=0.1mH,IAS =-41A

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.

Typical Characteristics

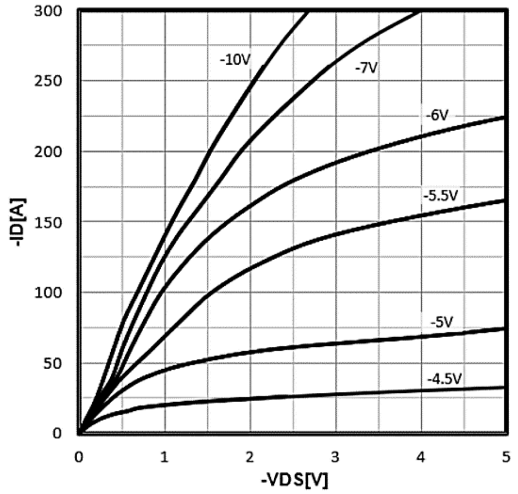


Figure 1. Type. Output Characteristics (Tj=25 ℃)

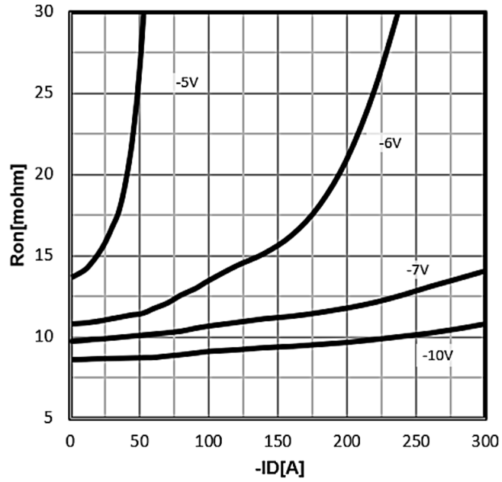


Figure 2. Type. drain-source on resistance

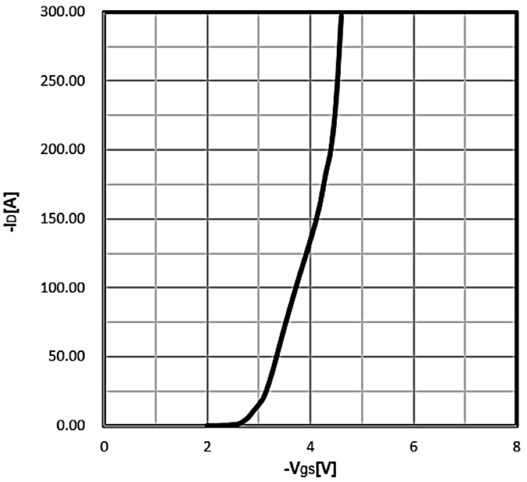


Figure 3. Type. transfer characteristics

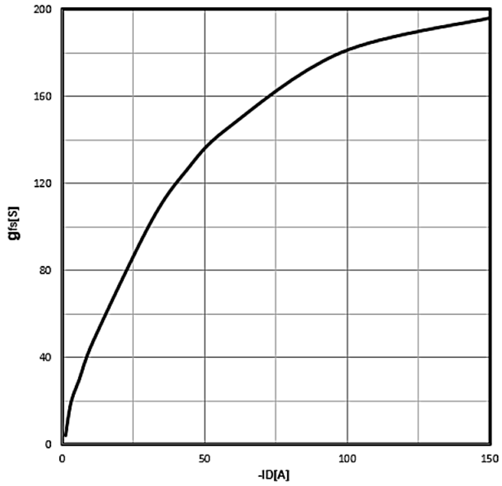


Figure 4. Type. forward transconductance

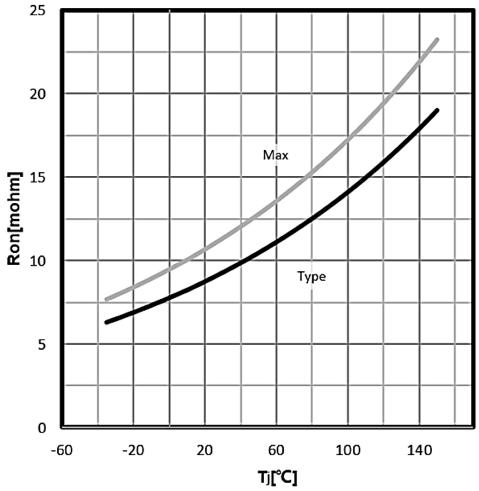


Figure 5. Drain-source on-state resistance
RDS(on) =f(Tj); ID =80A; VGS =10V

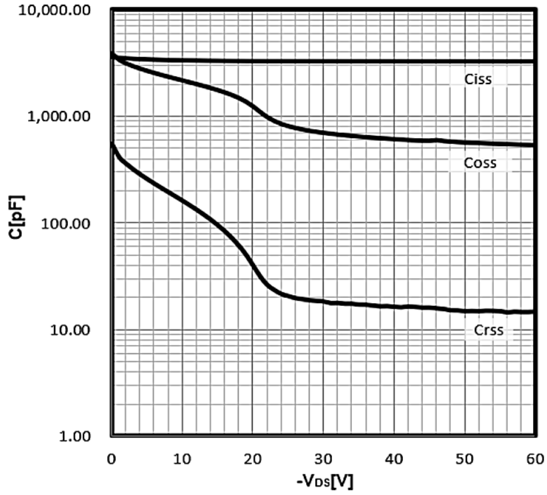


Figure 6 . Body-Diode Characteristics
C=f(VDS); VGS =0V; f=1MHz

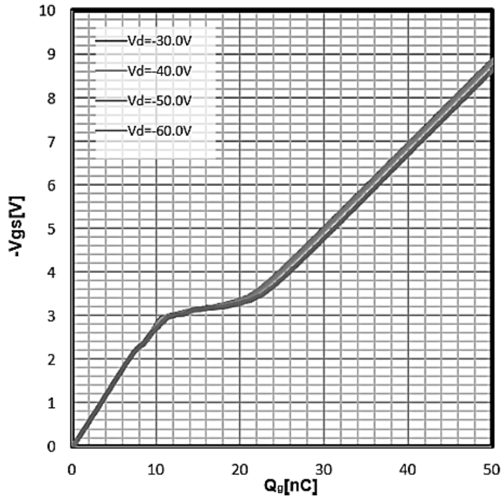


Figure 7. Typ. gate charge
VGS =f(Q gate) ; ID =20A

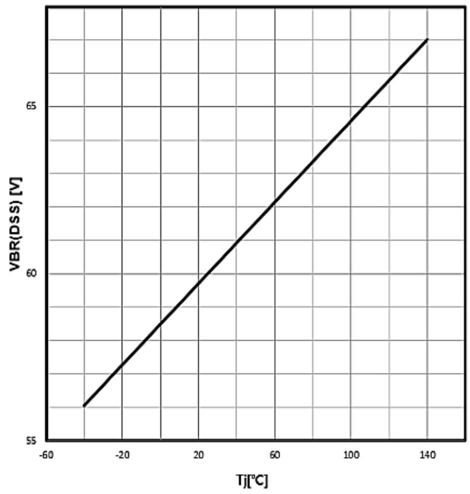


Figure 8. Drain Current Derating
VBR(DSS) =f(T j); I D =250uA

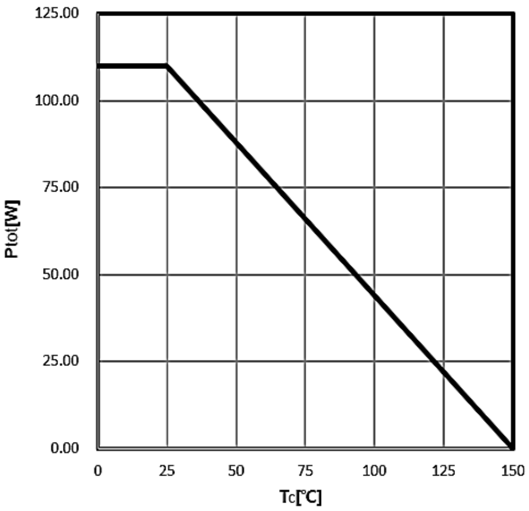


Figure 7. Power Dissipation

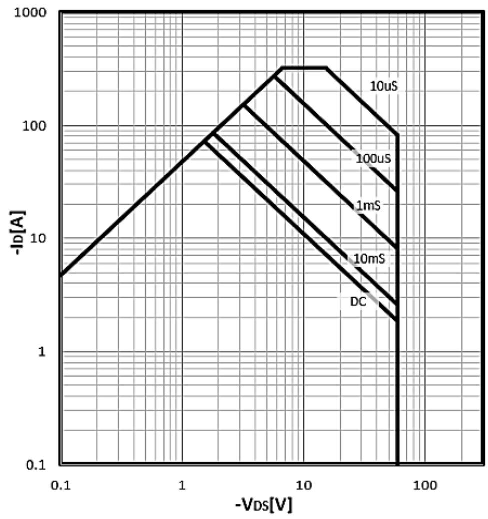


Figure 8. Safe operating area

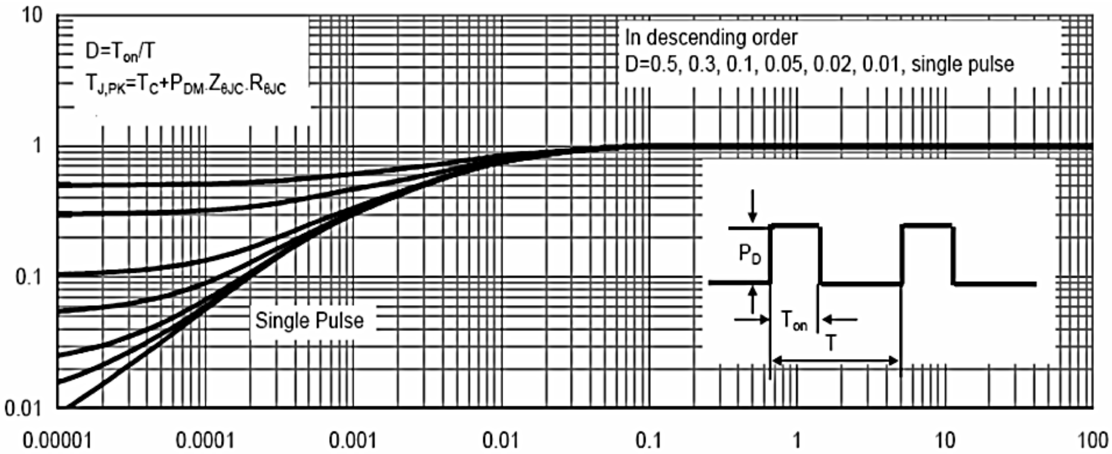
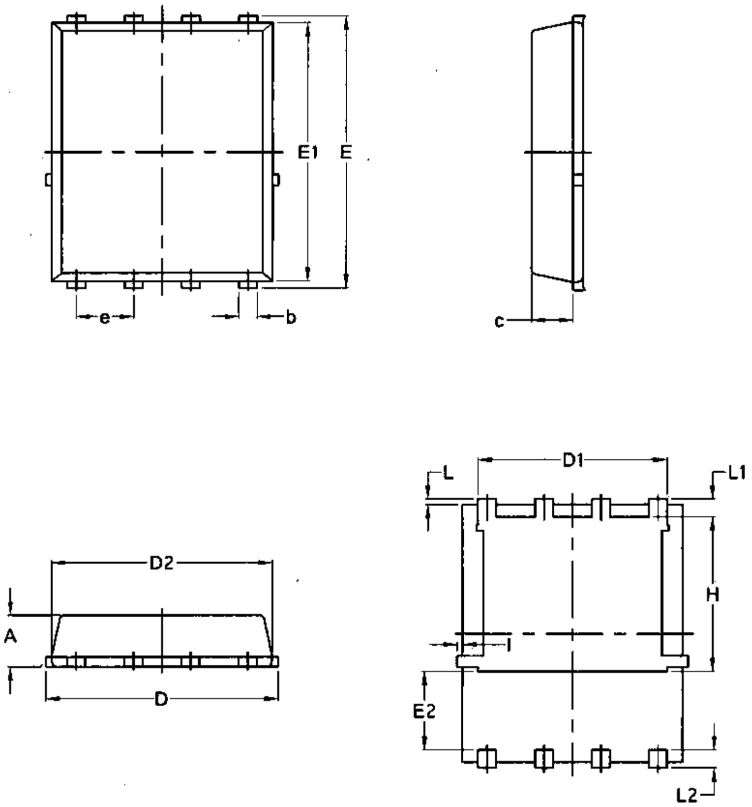


Figure 10. Max. transient thermal impedance

ZthJC =f(tp)

Package Mechanical Data-DFN5*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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