-40V P-Channel Enhancement Mode MOSFET

Description

TheXPX6P04AS uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

V_{DS} = -40V I_D =-6.0A

$R_{DS(ON)}$ < 63mΩ @ V_{GS}=-10V

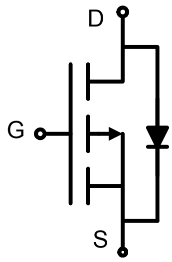
Application

Battery protection

Load switch

Uninterruptible power supply

SOT-23-3L top view



Schematic diagram

Product Information	Pack	Marking	Qty(PCS)
XPX6P04AS	SOT23-3L	6P40	3000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Steady State	Units
VDS	Drain-Source Voltage	-40	V
VGS	Gate-Source Voltage	±20	V
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ -4.5V[1]	-6.0	A
I_D@T_A=70℃	Continuous Drain Current, V_{GS} @ -4.5V[1]	-3.0	A
IDM	Pulsed Drain Current[2]	-16.1	A
P_D@T_A=25℃	Total Power Dissipation[3]	1.32	W
P_D@T_A=70℃	Total Power Dissipation[3]	0.84	W
TSTG	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
$R_{\theta}JA$	Thermal Resistance Junction-Ambient [1]	125	℃/W
$R_{\theta}JC$	Thermal Resistance Junction-Case[1]	80	℃/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-40	-46	---	V
△BVDSS/△TJ	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.018	---	V/℃
RDS(ON)	Static Drain-Source On-Resistance[2]	V_{GS}=-4.5V , I_D=-3A	---	65	72	mΩ
		V_{GS}=-2.5V , I_D=-2A	---	89	100	
VGS(th)	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-1.0	-1.5	-2.5	V
△$V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	2.5	---	mV/℃
IDSS	Drain-Source Leakage Current	V_{DS}=-24V , V_{GS}=0V ,T_J=25℃	---	---	-1	uA
		V_{DS}=-24V , V_{GS}=0V ,T_J=55℃	---	---	-5	
IGSS	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-3A	---	5.8	---	S
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-32V , V_{GS}=-4.5V , I_D=-3A	---	6.4	---	nC
Qgs	Gate-Source Charge		---	2.1	---	
Qgd	Gate-Drain Charge		---	2.5	---	
Td(on)	Turn-On Delay Time	V_{DD}=-20V , V_{GS}=-4.5V , R_G=3.3Ω, I_D=-3A	---	4.2	---	ns
T_r	Rise Time		---	23	---	
Td(off)	Turn-Off Delay Time		---	26.8	---	
T_f	Fall Time		---	20.6	---	
Ciss	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	620	---	pF
Coss	Output Capacitance		---	65	---	
Crss	Reverse Transfer Capacitance		---	53	---	
IS	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	-5.2	A
ISM	Pulsed Source Current[2,4]		---	---	-16.1	A
VSD	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1	V

Note :

1、The data tested by surface mounted on a 1 inch FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The power dissipation is limited by 150℃ junction temperature

4、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

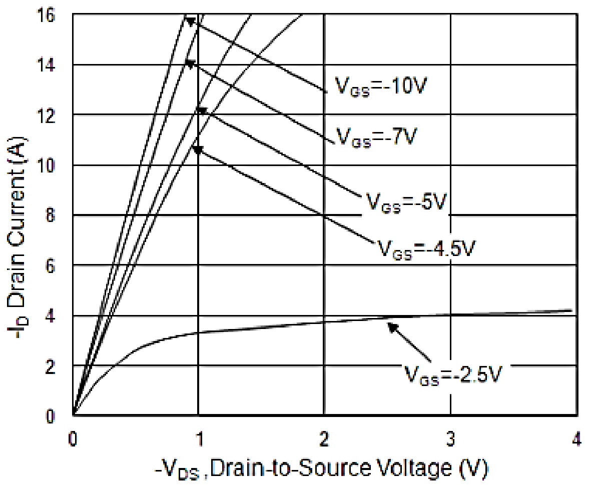


Fig.1 Typical Output Characteristics

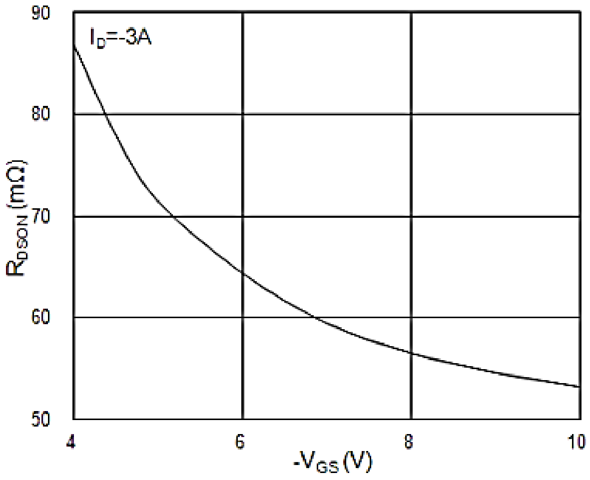


Fig.2 On-Resistance vs. G-S Voltage

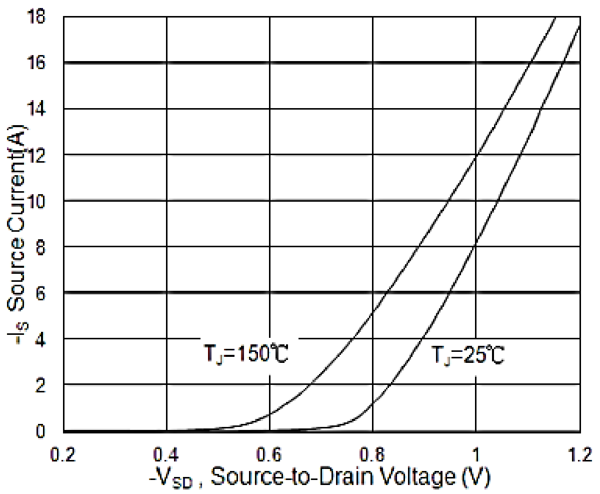


Fig.3 Forward Characteristics Of Reverse

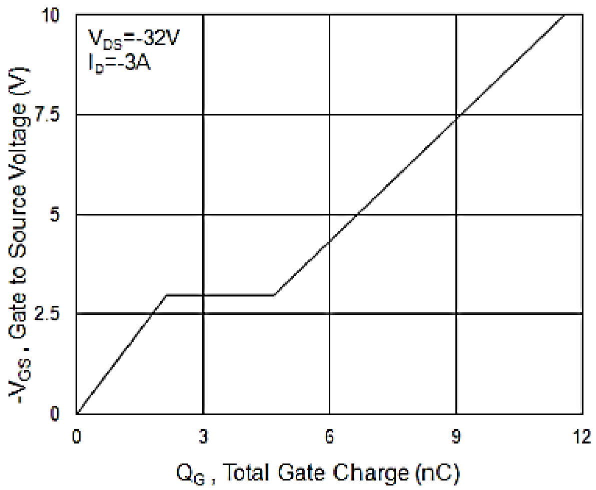


Fig.4 Gate-Charge Characteristics

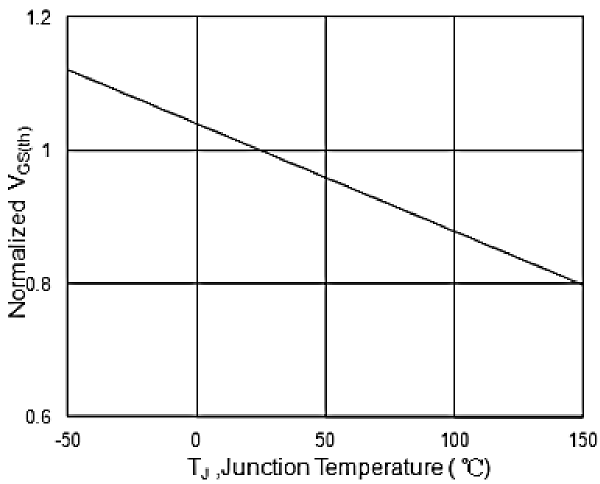


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

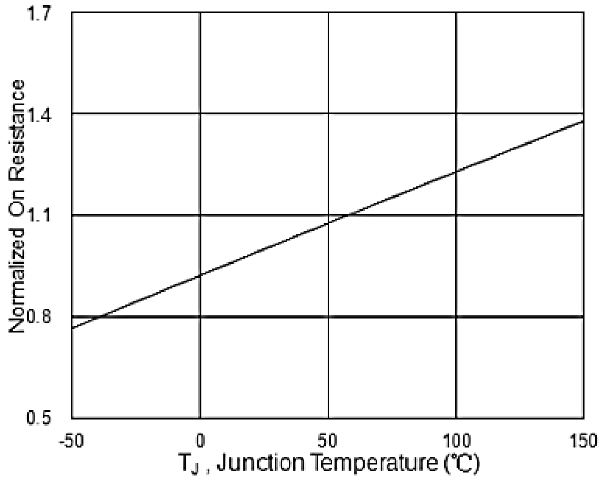


Fig.6 Normalized R_{DSON} vs. T_J

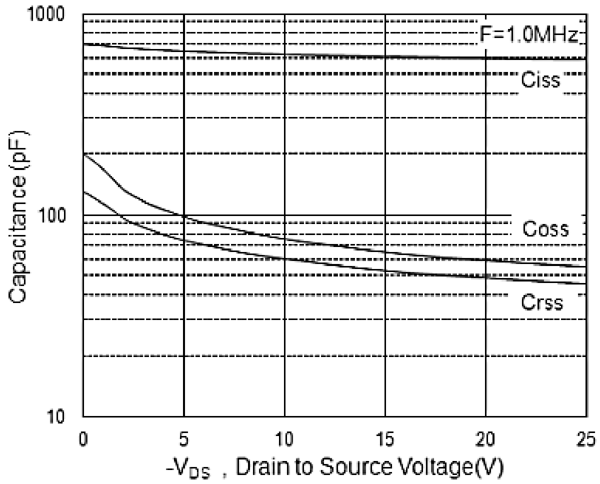


Fig.7 Capacitance

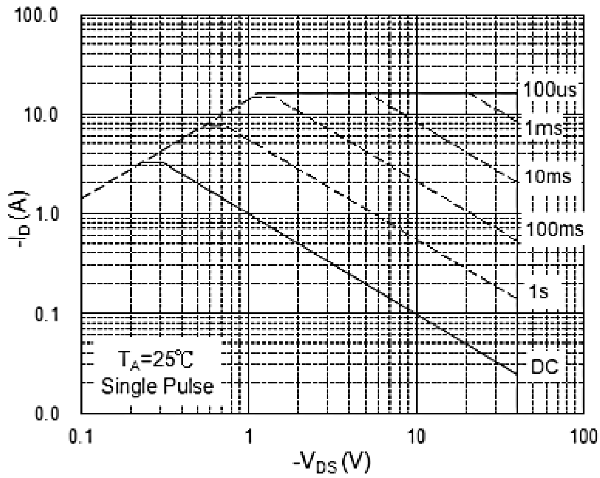


Fig.8 Safe Operating Area

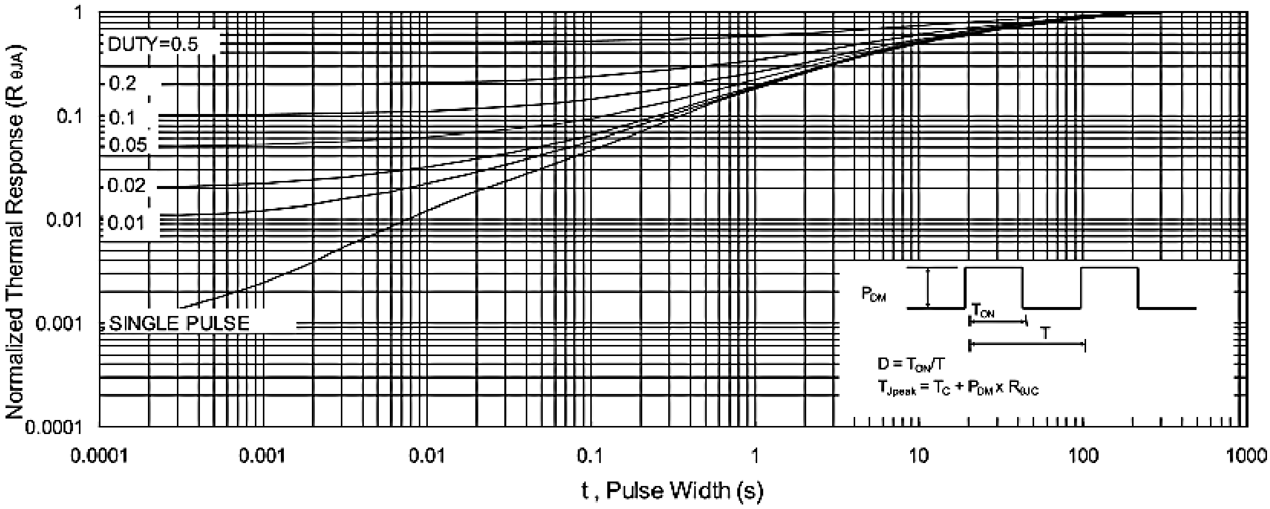


Fig.9 Normalized Maximum Transient Thermal Impedance

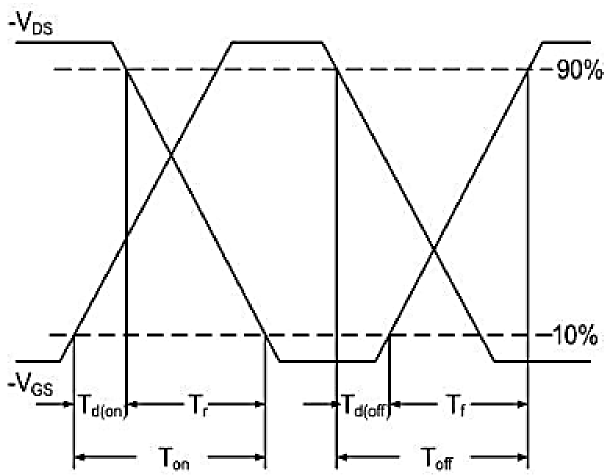


Fig.10 Switching Time Waveform

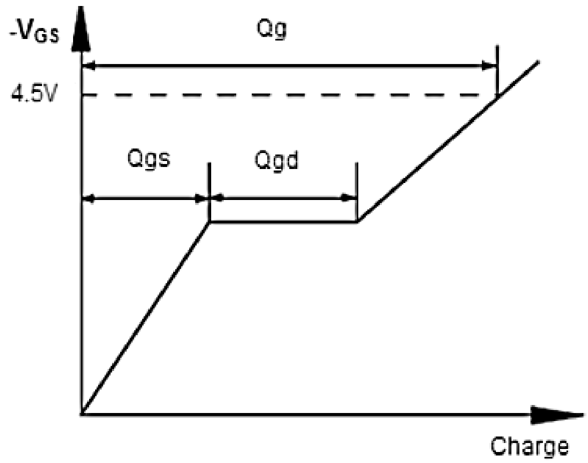
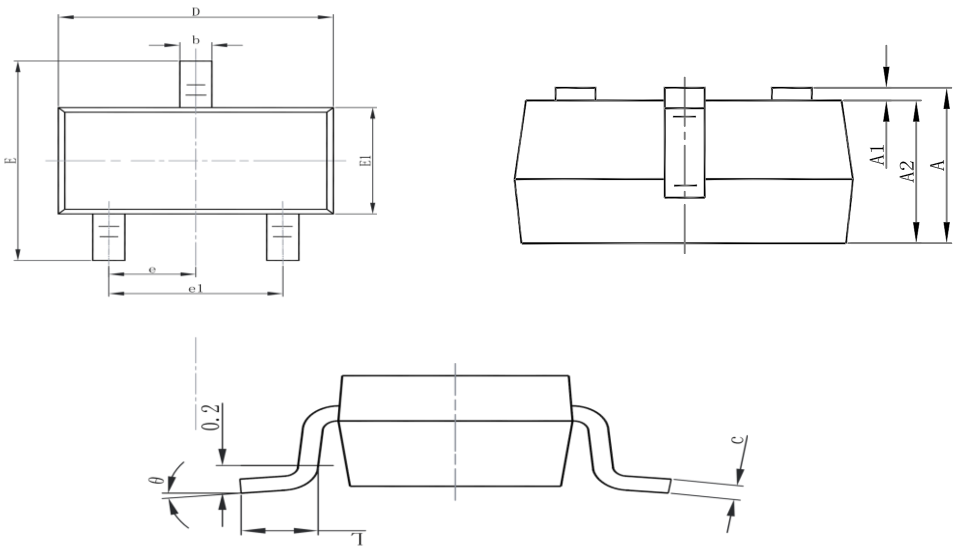


Fig.11 Gate Charge Waveform

Package Mechanical Data:SOT23-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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